SPECTRUM
SYSTEMENTWICKLUNG MICROELECTRONIC GMBH

M2i.30xx - 12 bit transient recorder up to 200 MS/s

- **PCI-X interface (100% compatible to PCI)**
- **Fastest 12 bit A/D converter board**
- **Up to 200 MS/s on one channel, 100 MS/s on two channels or 60 MS/s on four channels**
- **Simultaneously sampling on all channels**
- **Separate ADC and amplifier per channel**
- **6 input ranges: ±200 mV up to ± 10 V**
- **Up to 2 GSample (4 GByte) on-board memory**
- **Sustained streaming mode up to 200 MB/s**
- **Window, pulse width, re-arm, OR/AND trigger**
- **Programmable input offset of ±100%**
- **Synchronization option available for up to 16 cards**
- **Options: synchronous digital channels, ABA mode**



Product range overview

All boards of the M2i.30xx series may use the whole installed on-board memory for the currently activated number of channels.

Model	1 channel	2 channels	4 channels
M2i.3010	80 MS/s		
M2i.3011	40 MS/s	40 MS/s	
M2i.3012	80 MS/s	40 MS/s	
M2i.3013	40 MS/s	40 MS/s	40 MS/s
M2i.3014	80 MS/s	80 MS/s	40 MS/s
M2i.3015	160 MS/s	80 MS/s	
M2i.3016	160 MS/s	80 MS/s	40 MS/s
M2i.3020	100 MS/s		
M2i.3021	50 MS/s	50 MS/s	
M2i.3022	100 MS/s	50 MS/s	
M2i.3023	50 MS/s	50 MS/s	50 MS/s
M2i.3024	100 MS/s	100 MS/s	50 MS/s
M2i.3025	200 MS/s	100 MS/s	
M2i.3026	200 MS/s	100 MS/s	50 MS/s
M2i.3027	100 MS/s	100 MS/s	
M2i.3031	60 MS/s	60 MS/s	
M2i.3033	60 MS/s	60 MS/s	60 MS/s

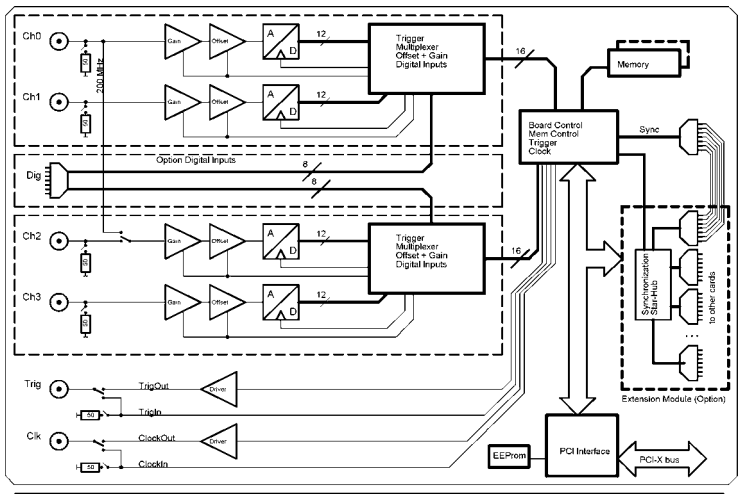
General Information

The 17 models of the M2i.30xx series are designed for the fast and high quality data acquisition. Each of the up to four input channels has its own A/D converter and its own programmable input amplifier. This allows to record signals simultaneously on all channels with 12 bit resolution without any phase delay between them.

The extremely large on-board memory allows long time recording even with the highest sampling rates. A FIFO mode is also integrated on the board. This allows the acquisition of data continuously for online processing or for data storage to hard disk.

- Completely new developed base card
- 4 GByte memory with one slot width
- Optimized low jitter clock section
- Multi, Gate with programmable pre, posttrigger and timestamp
- Zero phase delay synchronization
- AND/OR conjunction of trigger/gate

Hardware block diagram



Software programmable parameters

Input Range	±200 mV, ±500 mV, ±1 V, ±2 V, ±5 V, ±10 V
Input impedance	50 Ohm / 1 MOhm
Input Offset	±100% of input range in steps of 1%
Clock mode	Int. PLL, int. quartz, ext. clock, ext. divided, ext. reference clock, sync
Clock impedance	50 Ohm / high impedance (> 4kOhm)
Trigger impedance	50 Ohm / high impedance (> 4kOhm)
Trigger mode	Channel, Extern, SW, Auto, Window, Pulse, Re-Arm, Or/And, Delay
Trigger level	10 bit resolution: 1/1024 to 1023/1024 of input range
Trigger edge	Rising edge, falling edge or both edges
Trigger pulse width	0 to [64k - 1] samples in steps of 1 sample
Trigger delay	0 to [64k - 1] samples in steps of 1 sample
Memory depth	8 up to [installed memory / number of active channels] in steps of 4
Posttrigger	4 up to [8G - 4] samples in steps of 4
Multiple Recording segment size	8 up to[installed memory / 2 / active channels] in steps of 4
Multi / Gated pretrigger	0 up to [8k samples / number of active channels - 16]
ABA clock divider	1 up to [64k - 1] in steps of 1
Synchronization clock divider	2 up to [8k - 2] in steps of 2
Channel selection	Any 1, 2 or 4 channels (see manual for clock limits on the selections)

Application examples

LDA/PDA	Production test	Laboratory equipment
Radar	Spectroscopy	Test of mobile communication
Ultrasound	Medical equipment	Sonar

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Software Support

Windows drivers

The cards are delivered with drivers for Windows 2000, Windows XP, Windows XP64 and Windows Vista (Beta). Programming examples for Visual C/C++, Borland C++ Builder, Gnu C, LabWindows/CVI, Borland Delphi and Visual Basic are included.

Linux Drivers



All cards are delivered with full Linux support. Pre compiled kernel modules are included for the most common distributions like RedHat, Suse or Debian. The linux support is enhanced by SMP support, versatile programming examples as well as the possibility to get the driver sources for own compilation.

SBench

A full licence of SBench the easy-to-use graphical operating software for the Spectrum cards is included in the delivery. The version 6 is running under Windows as well as under Linux (KDE and GNOME).

Third-party products

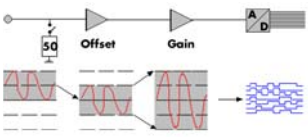
A lot of third-party products are supported as an option. Choose between LabVIEW, MATLAB, DASYLab and Agilent VEE. All drivers come with examples and detailed documentation.

MI Software compatibility layer

To allow an easy change from MI cards to the new M2i cards for existing software a special software compatibility layer is delivered with the cards. This DLL converts MI calls to M2i calls and simulates a MI card in the software.

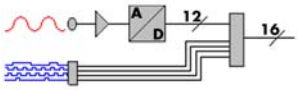
Hardware features and options

Input Amplifier



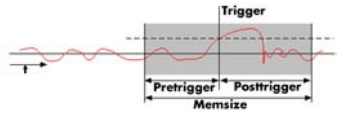
The analog inputs can be adapted to real world signals using a wide variety of settings that are individual for each channel. By using software commands the input termination can be changed between 50 Ohm and 1 MOhm, one can select a matching input range and the signal offset can be compensated for.

Digital inputs



This option acquires additional synchronous digital channels phase-stable with the analog data. When the option is installed there are 4 additional digital inputs for every analog A/D channel.

Ring buffer mode



The ring buffer mode is the standard mode of all oscilloscope boards. Data is written in a ring memory of the board until a trigger event is detected. After the event the posttrigger values are recorded. Because of this continuously recording into a ring buffer there are also samples prior to the trigger event visible: Pretrigger = Memsize - Posttrigger.

FIFO mode

The FIFO mode is designed for continuous data transfer between measurement board and PC memory (up to 225 MB/s on a PCI-X slot and up to 115 MB/s on a PCI slot) or hard disk. The control of the data stream is done automatically by the driver on interrupt request. The complete installed on-board memory is used for buffer data, making the continuous streaming extremely reliable.

Channel trigger

The data acquisition boards offer a wide variety of trigger modes. Besides the standard signal checking for level and edge as known from oscilloscopes it's also possible to define a window trigger. All trigger modes can be combined with the pulsewidth trigger. This makes it possible to trigger on signal errors like too long or too short pulses. In addition to this a re-arming mode (for accurate trigger recognition on noisy signals) the AND/OR conjunction of different trigger events is possible. As a unique feature it is possible to use deactivated channels as trigger sources.

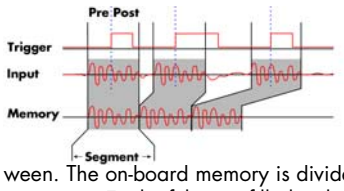
External trigger I/O

All boards can be triggered using an external TTL signal. It's possible to use positive or negative edge also in combination with a programmable pulse width. An internally recognised trigger event can - when activated by software - be routed to the trigger connector to start external instruments.

Pulse width

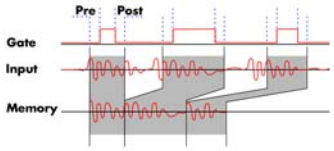
Defines the minimum or maximum width that a trigger pulse must have to generate a trigger event. Pulse width can be combined with channel trigger, pattern trigger and external trigger.

Multiple Recording



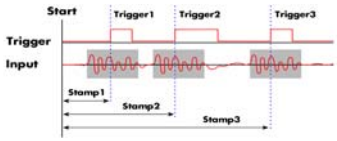
The Multiple Recording option allows the recording of several trigger events with an extremely short re-arming time. The hardware doesn't need to be restarted in between. The on-board memory is divided in several segments of the same size. Each of them is filled with data if a trigger event occurs. Pre- and posttrigger of the segments can be programmed. The number of acquired segments is only limited by the used memory and is unlimited when using FIFO mode.

Gated Sampling



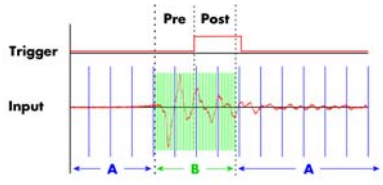
The Gated Sampling option allows data recording controlled by an external gate signal. Data is only recorded if the gate signal has a programmed level. In addition a pre-area before start of the gate signal as well as a post area after end of the gate signal can be acquired. The number of gate segments is only limited by the used memory and is unlimited when using FIFO mode.

Timestamp



The timestamp option writes the time positions of the trigger events in an extra memory. The timestamps are relative to the start of recording, a defined zero time, externally synchronised to a radio clock, or a GPS receiver. With this option acquisitions of systems on different locations can be set in a precise time relation.

ABA mode

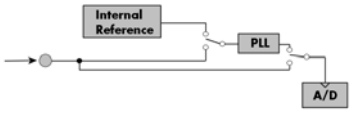


The optional ABA mode combines slow continuous data recording with fast acquisition on trigger events. The ABA mode works like a slow data logger combined with a fast digitizer. The exact position of the trigger events is stored as timestamps in an extra memory.

External clock I/O

Using a dedicated connector a sampling clock can be fed in from an external system. It's also possible to output the internally used sampling clock to synchronise external equipment to this clock.

Reference clock



The option to use a precise external reference clock (normally 10 MHz) is necessary to synchronise the board for high-quality measurements with external equipment (like a signal source). It's also possible to enhance the quality of the sampling clock in this way. The driver automatically generates the requested sampling clock from the fed in reference clock.

Star-Hub



The star-hub is an additional module allowing the phase stable synchronisation of up to 16 boards. Independent of the number of boards there is no phase delay between all channels. The star-hub distributes trigger and clock information between all boards. As a result all connected boards are running with the same clock and the same trigger. All trigger sources can be combined with OR/AND allowing all channels of all cards to be trigger source at the same time. The star-hub is available as 5 card and 16 card version. The 5 card version doesn't need an extra slot.

Technical Data

Analog Inputs

Resolution	12 bit
Differential non linearity (DNL)	≤ 1 LSB (ADC)
Integral non linearity (INL)	≤ 1 LSB (ADC)
Offset error	can be calibrated by user
Gain error	< 1% of current value
Programmable input offset	±100% of current input range
Crosstalk 1 MHz signal, 50 Ohm term	< -70 dB between any adjacent channels
Input signal with 50 Ohm termination	max 5 V rms
Analog Input impedance	50 Ohm / 1 MOhm || 25 pF
Over voltage protection (range ≤ ±1 V)	±5 V
Over voltage protection (range > ±1 V)	±50 V
Connector (analog and trigger/clock)	3 mm SMB male

Trigger

Multi, Gate: re-arming time	<4 Samples
Max Pretrigger at Multi, Gate, FIFO	8176 Samples as sum of all active channels
Internal trigger accuracy	1 Sample
Channel trigger resolution	10 bits
Trigger output delay	One positive edge after internal trigger event
External trigger type	TTL compatible
External trigger input	Low ≤ 0.8 V, High ≥ 2.0 V, ≥ 2 clock periods
External trigger maximum voltage	-0.5 V up to +5.5 V
External trigger accuracy (≤100 MS/s)	1 Sample
External trigger accuracy (>100 MS/s)	2 Samples
External trigger output levels	Low ≤ 0.4 V, High ≥ 2.4 V, TTL compatible
External trigger output drive strength	Capable of driving 50 ohm load

Power consumption (max speed)	**3,3 V**	**5 V**	**-12 V**	**+12 V**	**Total**
M2i.30x0 (32 MS memory)	2.2 A	0.8 A	n.u.	n.u.	11,3 W
M2i.30x1, x2 (32 MS memory)	2.3 A	0.9 A	n.u.	n.u.	12,1 W
M2i.30x5, x7 (32 MS memory)	2.5 A	1.1 A	n.u.	n.u.	13,8 W
M2i.30x3, x4, x6 (32 MS memory)	2.6 A	1.4 A	n.u.	n.u.	15,6 W
M2i.3026 (2 GS memory), max. power	3.7 A	1.4 A	n.u.	n.u.	19,3 W

Certifications and Compliances

EMC Immunity	Compliant with CE Mark
EMC Emission	Compliant with CE Mark

Clock

Internal clock range (PLL mode)	1 kS/s to max (see table below)
Internal clock accuracy	20 ppm
Internal clock: max. jitter in PLL mode	TBD
Internal clock: max. jitter in quartz mode	TBD
Internal clock setup granularity (≤ 100 M)	≤1% of range (100M, 10M, 1M, 100k,...)
Internal clock setup granularity example	range 1M to 10M: stepsize ≤ 100k
Internal clock setup granularity (> 100 M)	one fixed value (160 MS/s or 200 MS/s)
Reference clock: external clock range	≥ 4.0 MHz and ≤ 125.0 MHz
External clock range	1 MS/s to max (see table below)
External clock delay to internal clock	5,4 ns
External clock input	Low ≤ 0.8 V, High ≥ 2.0 V, duty 45% - 55%
External clock maximum voltage	-0.5 V up to +5.5 V
External clock output levels	Low ≤ 0.4 V, High ≥ 2.4 V, TTL compatible
External clock output drive strength	Capable of driving 50 ohm load

Digital Inputs (Option)

Digital inputs: input impedance	110 Ohm @ 2.5V
Digital inputs delay to analog sample	-11 Samples
Maximum voltage	-0.3 V up to +5.5 V
Input voltage	Low ≤ 0.8 V, High ≥ 2.0 V
Connector (digital inputs)	40 pole half pitch (Hirose FX2 series)

BaseXIO (Option)

BaseXIO Connector (extra bracket)	8 x SMB (8 x MMCX internal)
BaseXIO input	TTL compatible: Low ≤ 0.8 V, High ≥ 2.0 V
BaseXIO input maximum voltage	-0.5 V up to +5.5 V
BaseXIO output levels	TTL compatible: Low ≤ 0.4 V, High ≥ 2.4 V
BaseXIO output drive strength	32 mA maximum current

Environmental and Physical details

Dimension (PCB only)	312 mm x 107 mm (full PCI length)
Width (Standard or star-hub 5)	1 full size slot
Width (star-hub 16)	2 full size slots
Width (with digital inputs)	1 full size slots + 1 half size slot
Weight (depending on options/channels)	290g (2 ch) up to 460g (4 ch + dig + sh)
PCI / PCI-X bus slot compatibility	32 bit or 64 bit, 33 MHz up to 133 MHz
Warm up time	10 minutes
Operating temperature	0°C - 50°C
Storage temperature	-10°C - 70°C
Humidity	10% to 90%

Dynamic Parameters

	M2i.3011 M2i.3013		M2i.3021 M2i.3023		M2i.3031 M2i.3033		M2i.3010 M2i.3012 M2i.3014		M2i.3020 M2i.3022 M2i.3024 M2i.3027		M2i.3015 M2i.3016		M2i.3025 M2i.3026	
max internal clock	40 MS/s		50 MS/s		62.5 MS/s		80 MS/s		105 MS/s		160 MS/s		200 MS/s	
max external clock	40 MS/s		50 MS/s		62.5 MS/s		80 MS/s		105 MS/s		80 MS/s		105 MS/s	
-3 dB bandwidth	DC to 20 MHz		DC to 25 MHz		DC to 30 MHz		DC to 40 MHz		DC to 40 MHz		DC to 40 MHz		DC to 40 MHz	
Zero noise level (< 125 MS/s)	< 1.1 LSB rms		< 1.1 LSB rms		TBD		TBD		< 1.2 LSB rms		TBD		TBD	
Zero noise level (> 125 MS/s)	n.a.		n.a.		n.a.		n.a.		n.a.		TBD		TBD	
Test - sampling rate	40 MS/s		50 MS/s		60 MS/s		80 MS/s		100 MS/s		80 MS/s		100 MS/s	
Test signal frequency	1 MHz	4 MHz	1 MHz	4 MHz	1 MHz	4 MHz	1 MHz	9 MHz	1 MHz	9 MHz	1 MHz	9 MHz	1 MHz	9 MHz
SNR (typ) (dB)	66.2	64.8	65.8	64.5	TBD	TBD	TBD	TBD	65.5	64.0	TBD	TBD	TBD	TBD
THD (typ) (dB)	-72.0	-71.0	-72.0	-71.0	TBD	TBD	TBD	TBD	-72.0	-66.1	TBD	TBD	TBD	TBD
SFDR (typ), excl. harm. (dB)	80.8	78.9	80.2	78.0	TBD	TBD	TBD	TBD	78.0	77.5	TBD	TBD	TBD	TBD
ENOB based on SNR (LSB)	10.7	10.4	10.7	10.4	TBD	TBD	TBD	TBD	10.6	10.3	TBD	TBD	TBD	TBD
ENOB based on SINAD (LSB)	10.6	10.2	10.6	10.2	TBD	TBD	TBD	TBD	10.4	10.1	TBD	TBD	TBD	TBD

Dynamic parameters are measured at ± 1 V input range (if no other range is stated) and 50 Ohm termination with the samplerate specified in the table. Measured parameters are averaged 20 times to get typical values. Test signal is a pure sine wave of the specified frequency with > 99% amplitude. SNR and RMS noise parameters may differ depending on the quality of the used PC. SNR = Signal to Noise Ratio, THD = Total Harmonic Distortion, SFDR = Spurious Free Dynamic Range, SINAD = Signal Noise and Distortion, ENOB = Effective Number of Bits. For a detailed description please see application note 002.

Order Information

Versions

Order no.	1 channel	2 channels	4 channels
M2i.3010	80 MS/s		
M2i.3011	40 MS/s	40 MS/s	
M2i.3012	80 MS/s	40 MS/s	
M2i.3013	40 MS/s	40 MS/s	40 MS/s
M2i.3014	80 MS/s	80 MS/s	40 MS/s
M2i.3015	160 MS/s	80 MS/s	
M2i.3016	160 MS/s	80 MS/s	40 MS/s
M2i.3020	100 MS/s		
M2i.3021	50 MS/s	50 MS/s	
M2i.3022	100 MS/s	50 MS/s	
M2i.3023	50 MS/s	50 MS/s	50 MS/s
M2i.3024	100 MS/s	100 MS/s	50 MS/s
M2i.3025	200 MS/s	100 MS/s	
M2i.3026	200 MS/s	100 MS/s	50 MS/s
M2i.3027	100 MS/s	100 MS/s	
M2i.3031	60 MS/s	60 MS/s	
M2i.3033	60 MS/s	60 MS/s	60 MS/s

Memory

Order no.	Option
M2i.xxxx-64MS	Memory upgrade to 64 MSample (128 MB) total memory
M2i.xxxx-128MS	Memory upgrade to 128 MSample (256 MB) total memory
M2i.xxxx-256MS	Memory upgrade to 256 MSample (512 MB) total memory
M2i.xxxx-512MS	Memory upgrade to 512 MSample (1 GB) total memory
M2i.xxxx-1GS	Memory upgrade to 1 GSample (2 GB) total memory
M2i.xxxx-2GS	Memory upgrade to 2 GSample (4 GB) total memory

Options

Order no.	Option
M2i.xxxx-mr	Option Multiple Recording
M2i.xxxx-mgt	Option pack including Multiple Recording, Gated Sampling, Timestamp
M2i.xxxx-mgtab	Option pack including Multiple Recording, Gated Sampling, Timestamp, ABA mode
M2i.xxxx-SH5 (1)	Synchronization Star-Hub for up to 5 cards, only 1 slot width
M2i.xxxx-SH16 (1)	Synchronization Star-Hub for up to 16 cards
M2i.3xxx-dig	Additional synchronous digital inputs (4 per analog channel) including Cab-d40-idc-100
M2i.xxxx-bxio	Option BaseXIO: 8 digital I/O lines usable as asynchronous I/O, timestamp ref-clock and additional external trigger lines, additional bracket with 8 SMB connectors

Cables

Order no.	Option
Cab-3f-9m-80	Adapter cable SMB female to BNC male, 80 cm
Cab-3f-9f-80	Adapter cable SMB female to BNC female, 80 cm
Cab-3f-3f-80	Adapter cable SMB female to SMB female, 80 cm
Cab-3f-9m-200	Adapter cable SMB female to BNC male, 200 cm
Cab-3f-9f-200	Adapter cable SMB female to BNC female, 200 cm
Cab-3f-3f-200	Adapter cable SMB female to SMB female, 200 cm
Cab-3f-9f-5	Adapter cable SMB female to BNC female, 5 cm (short cable especially for oscilloscopes probes)
Cab-d40-idc-100	Flat ribbon cable 40 pole FX2 for digital connector to 2x20 pole IDC connector, 100 cm
Cab-d40-d40-100	Flat ribbon cable 40 pole FX2 for digital connector to 40 pole digital FX2 connector, 100 cm

Drivers

Order no.	Option
M2i.xxxx-ml	MATLAB driver for all M2i cards
M2i.30xx-lv	LabVIEW driver for all M2i.30xx cards
M2i.30xx-dl	DASYLab driver for all M2i.30xx cards
M2i.30xx-vee	Agilent VEE driver for all M2i.30xx cards

(1) : Just one of the options can be installed at a time.

technical changes and printing errors possible