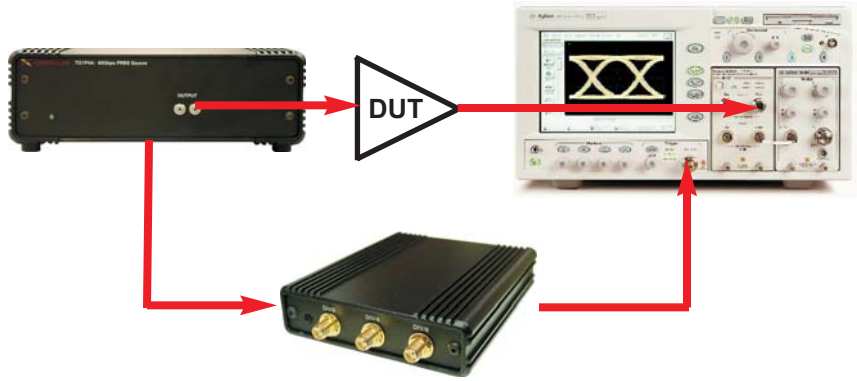
TG1P4A Datasheet

22 - 44Gbps PRBS SOURCE





Driver Amplifier Test Set-up

Shown above is a typical measurement setup for measuring modulator driver amplifiers. Included is a divide by 8 (TD40MCA) for scope triggering.

Features

- Self-contained PRBS Generator
- 22 to 44 Gbps data rates
- Built-in oscillator (39.8 Gb/s)
- 2e7, 2e15, and 2e31 patterns
- 1.2 V differential output
- Ultra low noise trigger provided (20 GHz) for precision time base applications
- External clock input
- Ultra-low jitter
  - <3 ps p-p
  - 400 fs rms
- Centellax Divider module for low frequency trigger inputs.
- Pattern trigger output
- Centellax Driver Amplifiers optional for higher output swing (>3V or >7V)
- Small size (7" x 10" x 2.5")

Description

The Centellax 22-44Gbps PRBS Source is a fully self-contained 40 Gbps pattern generator. This product has been designed to provide an excellent quality “EYE” at a fraction of the price of current market solutions. This is made possible through comprehensive integration of the key building blocks into monolithic integrated circuits founded on SiGe technology. The performance generated from the 22-44Gbps PRBS Source is world class with the typical EYE having <3 ps p-p jitter, 600 mV of output swing and <7 ps rise time.

All of this comes in a package one sixth the size of any other solution on the market which allows you to put your source directly at your device under test regardless of your lab bench environment.

Application

The Centellax 22-44Gbps PRBS Source is designed to be used as the source for testing ultra-high speed communications components such as those used in OC 768 / STM 256 applications. The 22-44Gbps PRBS Source is a perfect companion to a Digital Communication Analyzer in a stimulus response measurement for 40 Gbps components such as driver amplifiers, transimpedance amplifiers, optical modulators, and DEMUX. Other applications include backplane signal integrity testing, and cable testing.

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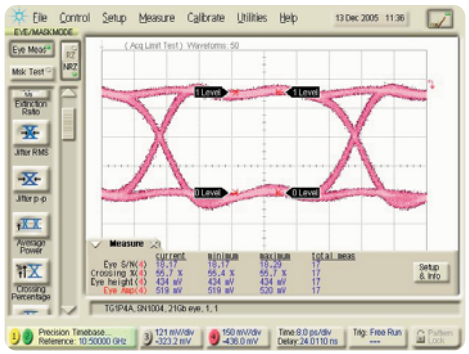
TG1P4A Datasheet



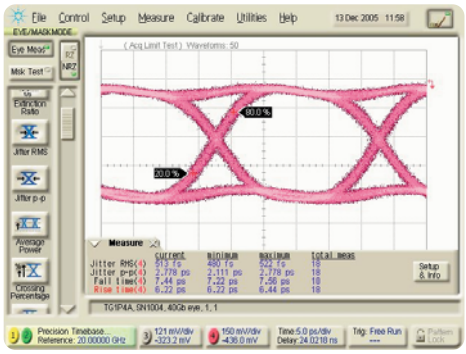
FRONT OF TG1P4A



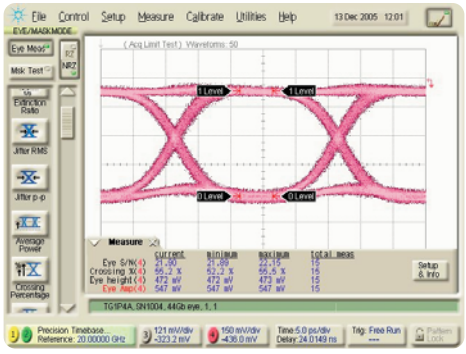
BACK OF TG1P4A
Showing the pattern control switches, clock inputs and outputs, and trigger outputs.



22 Gb/s



40 Gb/s



44 Gb/s

Label	Description
Power	Power Switch on/off
Clk Input	External Clock Input (11 - 22GHz)
Clk Output	Internal Clock Output (19.9 GHz)
Clk / 1	'Clk Input' Output
Reset	Reset / PRBS Pattern
Pattern Trigger	Pattern Trigger Output
Pattern Length	Pattern Selector

Logic	Pattern	Polynomial Description
1 1	$2^{31} - 1$	$1 + x^{28} + x^{31}$
1 0	$2^{15} - 1$	$1 + x^{14} + x^{15}$
0 0	$2^{7} - 1$	$1 + x^{4} + x^{7}$

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Performance Specification Table

	Description		Minimum	Typical	Maximum	Unit
DATA OUTPUT	Bit Rate	TG1P4A TG1P4A-OPT003	37 22	- -	44 44	Gbps Gbps
	RMS Jitter	TG1P4A TG1P4A-OPT003	- -	400 400	600 1000	fs fs
	Rise/Fall Times (20-80%)		-	6	8	ps
	Amplitude		500	550	600	mVpp
	SNR		-	18	-	
	Crossing		45	55	65	%
	Output Level	High Low	-50 -450	0 -	- -600	mV mV
CLOCK OUTPUT	Offset		-	0	-	V
	RMS Jitter		175	250	-	fs
	Amplitude		3.1	-	4	V
	Frequency		-	19.9	-	GHz
CLOCK INPUT	Input Level		13	-	16	dBm
	Offset		-	0	-	V
	Frequency		11	-	22	GHz
PATTERN TRIGGER OUTPUT	Output Level		-	800	-	mV
	Jitter		-	20	-	ps
CLK/1 OUTPUT	Output Level		1	-	4	dBm
PHASE ADJUSTMENT	Phase adjustment range		-	30	-	ps
PATTERN TRIGGER	Pulse Rate:	Freq (Input Clk) % Length (Pattern) % 32				
	Pulse Width:	$\frac{3}{\text{FREQ(Input Clk)}}$				

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