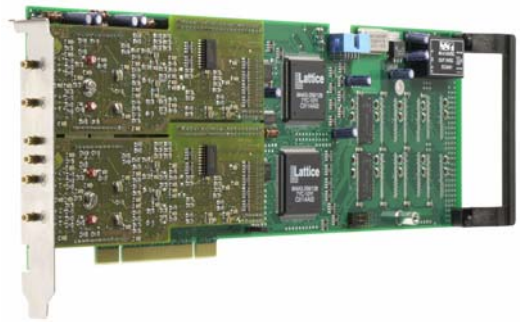
UltraFast

STRATEGIC TEST

# UF4500 - 16 bit high-speed data acquisition PCI cards

- **Standard PCI format**
- **Fastest 16 bit A/D converter board**
- **Maximum sampling rates: 200 kS/s, 500 kS/s or 1 MS/s on 2 or 4 channels**
- **Simultaneous sampling on all channels**
- **4 input ranges: ±1 V up to ± 10 V**
- **Differential / single-ended selectable**
- **Up to 256 MSample memory**
- **FIFO mode, up to 100 MB/s to PC**
- **Window and pulsewidth trigger**
- **Input offset up to ±100%**
- **Multi-card synchronization possible**
- **Windows program SBench 5.x included**



## Product range overview

| Model | 1 channel | 2 channels | 4 channels |
|---|---|---|---|
| UF.4520 | 200 kS/s | 200 kS/s | |
| UF.4521 | 200 kS/s | 200 kS/s | 200 kS/s |
| UF.4530 | 500 kS/S | 500 kS/s | |
| UF.4531 | 500 kS/s | 500 kS/s | 500 kS/s |
| UF.4540 | 1 MS/s | 1 MS/s | |
| UF.4541 | 1 MS/s | 1 MS/s | 1 MS/s |

## Software/Drivers

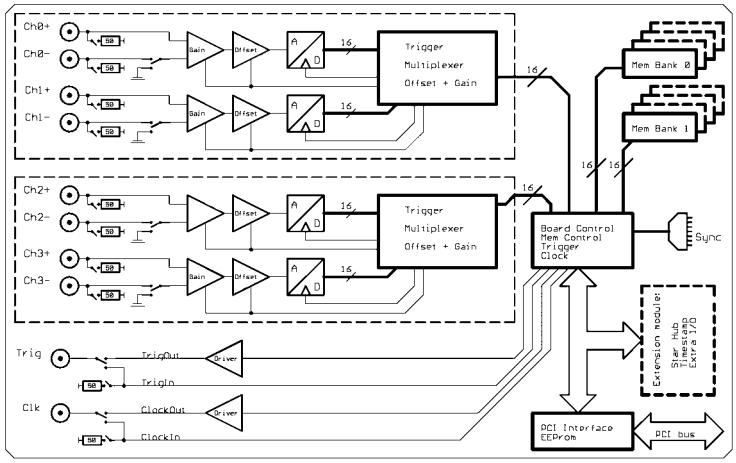
A wide variety of drivers and examples are delivered with the board or are available as an option:

- Windows 98/ME/NT/2000/XP - drivers
- Linux - drivers
- SBench 5.2
- Microsoft Visual C++ examples
- Borland Delphi examples
- Microsoft Visual Basic examples
- Microsoft Excel examples
- LabWindows/CVI examples
- FlexPro support with SBench
- LabVIEW - drivers (as option)
- DASYLab - drivers (as option)
- MATLAB - drivers (as option)
- Agilent VEE - drivers (as option)

## General Information

The UF4500 for the first time offers full 16 bit A/D resolution on all simultaneously sampled channels at very high sample rates. Every channel has its own amplifier and A/D converter that eliminates the problems of low-cost multiplexed systems, such as phase error between the channels or high crosstalk.
Each card is supplied with 8MSample of onboard memory, which can be expanded onboard to 256 MSamples. Measured signals can be stored to on-board memory or transferred in real-time to the PC using the FIFO mode.
Each input channel can be offset calibrated using the software. The boards have two or four channels and can also be configured as a multi-channel system of up to 16 boards using the UF4500 of other A/D, D/A and DIgital I/O cards in the UltraFast range.

## Hardware block diagram




## Software programmable parameters

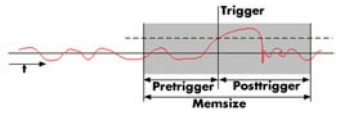
| | |
|---|---|
| Sample rate | 1 kS/s to max sample rate, external clock, ref clock |
| Input Range | ±1 V, ±2 V, ±5 V, ±10 V |
| Input impedance | 50 Ohm / 1 MOhm |
| Input type | Single-ended, differential |
| Input Offset | ±100% in steps of 1% |
| Clock impedance | 50 Ohm / 1 MOhm |
| Trigger impedance | 50 Ohm / 1 MOhm |
| Trigger mode | Channel, External, Software, Auto, Windows, Pulse |
| Trigger level | 1/256 to 255/256 of input range |
| Trigger edge | rising edge, falling edge or both edges |
| Trigger pulsewidth | 1 to 255 samples in steps of 1 sample |
| Memory depth | 32 up to installed memory in steps of 32 |
| Posttrigger | 32 up to 128 M in steps of 32 |

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Strategic Test Corporation · One Broadway · Cambridge · MA 02142 · USA · Toll-free Phn.: (866)898-FAST · Fax: (617)577-1209
Strategic Test Scandinavia AB · 184 84 Åkersberga-Stockholm · Sweden · Tel.: +46 (854)400 490 · Fax: +46 (854)080 554
Email: sales@strategic-test.com · www.strategic-test.com

## Possibilities and options

### Ring buffer mode




The ring buffer mode is the standard mode for all oscilloscope boards. Data is written in a ring memory on the board until a trigger event is detected. After the event the posttrigger values are recorded. Because the data is continuously recorded the pretrigger samples before the event are recorded also : Pretrigger = Memsize - Posttrigger.

### FIFO mode

The FIFO mode is designed for continuous data transfer between measurement board and PC memory (up to 100 MB /s) or hard disk (up to 50 MB/s). The data stream is controlled automatically by the driver on interrupt request.

### Channel trigger

The data acquisition boards offer a wide variety of trigger modes. In addition to the standard level and edge trigers found on traditional oscilloscopes, it is also possible to define a window trigger where the signal is inside or outside two defined amplitude limits. All trigger modes can be combined with the pulsewidth trigger which is similar to a time window. This is useful for eliminating false triggering due to noise spikes and can also be used to only capture short pulses.

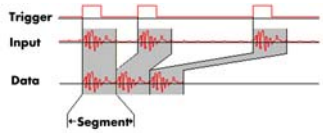
### External trigger I/O

All boards include an External Trigger connector for triggering using an external TTL signal. It is possible to use positive or negative edge and this may be combined with a programmable pulsewidth time window trigger. If triggering on a channel or by software, then this trigger event can be output though the external trigger connector to start external instruments.

### Pulse width

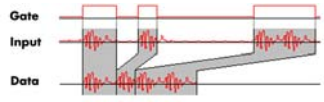
The pulsewidth trigger is similar to a time window. Once the time windows is defined, the pulsewidth trigger is combined with either the channel trigger, pattern trigger and external trigger.It is used to eliminate false triggerring due to noise spikes, but can also be used to capture short events only.

### Multiple Recording




The Multiple Recording option is used to record the signals from several trigger events without restarting the hardware. As a result it is possible to record a series of high speed signals, such as RADAR signals where several thousand may need to be captured in a short time. The user defines the number of waveforms to be recorded and the on-board memory is automatically divided in this number of equal-sized segments. Each segment is then filled with data as a trigger event occurs.

### Gated Sampling

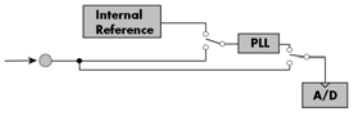



The Gated Sampling option ensures that data is only recorded to memory when the external gate signal reaches a pre-defined level. Effectively, this starts and stops the sampling clock. This option is typically used when you want to reduce the amount of data being recorded to only those signal segments of interest.

### External clock I/O

Each UltraFast board is supplied with an External Clock connector. This is used when you want to synchronize the board sampling rate with an external clock signal that may also synchronize other external instruments. It's also possible to output the board generated sampling clock to synchronise external equipment to the board.

### Reference clock




This option allows you to use a precise external reference clock (normally 10 MHz) in order to synchronize the board for high-quality measurements with external equipment (like a signal source). It's also possible to enhance the quality of the sampling clock this way. The driver automatically generates the requested sampling clock from the external reference clock signal.

### Cascading

The Cascading option is the easiest method to create multi-cards systems. Up to 4 UltraFast boards make be connected. The user is able to define the board that will generate the sampling rate clock which is then fed to the other boards. These other boards can subdivide the sampling rate if required using the onboard hardware divider. Similarly, one board is defined by the user as the trigger master. This board then transmits the trigger signals so that all boards start at the same time. There is a phase delay between two boards of about 500 pico seconds when this synchronisation option is used.

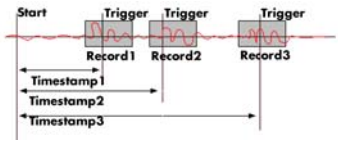
### Star Hub

The Star Hub is an additional daughterboard module that allows up to 16 UltraFast boards to be configured as a totally synchronized multi-card system. Unlike the Cascading option, there is no clock or trigger signal phase delay between the boards. The Star Hub module distributes the trigger and clock information between all boards so thatall connected boards are running with the exactly same clock and trigger; athough it is possible to use each boards programmable hardware divider to reduce the sampling rate on different boards.

### Extra I/O

The Extra I/O External module adds 24 additional digital I/O lines and 4 analog outputs to the UltraFast board. These additional channels are independent from the high-speed channels and can be controlled asynchronously. An additional PCI backpanel is supplied that houses these additional connectors. There is also an Extra I/O Internal version available with 16 digital I/O and 4 analog output channels. This version is intended for equipment manufacturers who need to route the cables inside the enclosure.

### Timestamp




The Timestamp option is used to record the effective time when trigger events occur, into a separate memory buffer. Each timestamp value is derived from the number of samples since the start of the measurement, to a defined zero time or externally synchronised to a radio clock or a GPS receiver. With this option measurements performed on systems at different locations can be synchronized.

### Input impedance

All inputs can be individually switched by software between 50 Ohm and 1 MOhm input impedance. If using fast signals and high sampling rates or you have 50 Ohm cable impedance, then the use of the 50 Ohm termination is recommended to minimise noise and signal reflections. If using weak signal sources or standard probes the use of the 1 MOhm termination is preferred.

### Differential inputs

With a simple software command the inputs could individually be switched from single-ended (in relation to ground) to differential. When the inputs are used in differential mode the A/D converter measures the difference between two lines with no relation to system ground.

## Technical Data

| | | | |
|---|---|---|---|
| Resolution | 16 bit | Dimension | 312 mm x 107 mm |
| Differential linearity error | < 1 LSB (ADC) | Width (Standard board) | 1 full size slot |
| Integral linearity error | < 2.5 LSB (ADC) | Width (with star hub option) | 2 full size slots |
| Multi: Trigger to 1st sample delay | fixed | Connector | 3 mm SMB male |
| Multi: Recovery time | < 20 samples | Inputs | Differential / Single Ended |
| ext. Trigger accuracy | 1 Sample | Input impedance | 50 Ohm / 1 MOhm \|\| 25 pF |
| int. Trigger accuracy | 1 Sample | Overvoltage protection | ±40 V |
| input signal with 50 ohm termination | max 5 V rms | Warm up time | 10 minutes |
| Trigger output delay | 1 Sample | Operating temperature | 0°C - 50°C |
| Offset errir | < 1 LSB, adjustable by user | Storage temperature | -10°C - 70°C |
| Gain error | < 1% | Humidity | 10% to 90% |
| Noise @ full speed, 50 ohm termination | < 2.5 LSB rms | | |
| Crosstalk @ 20 kHz | < -95 dB | Power consumption -12 V | max 100 mA (500 mWatt) |
| Ext. clock: delay to internal clock | 42 ns ± 2 ns | Power consumption +12 V | max 100 mA (500 mWatt) |
| Min internal clock | 1 kS/s | Power consumption 5 V @ full speed | max 1.8 A (9 Watt) |
| Min external clock | 1 kS/s | Power consumption 5 V @ power down | max 1.4 A (7 Watt) |

| | UF.4520<br>UF.4521 | UF.4530<br>UF.4531 | UF.4540<br>UF.4541 |
|---|---|---|---|
| max internal clock | 200 kS/s | 500 kS/s | 1 MS/s |
| max external clock | 200 kS/s | 500 kS/s | 1 MS/s |
| -3 dB bandwidth | >100 kHz | >250 kHz | >500 kHz |

## Dynamic Parameters

| | UF.4520<br>UF.4521 | UF.4530<br>UF.4531 | UF.4540<br>UF.4541 |
|---|---|---|---|
| Test - sample rate | 200 kS/s | 500 kS/s | 1 MS/s |
| Test signal frequency | 2 kHz | 2 kHz | 2 kHz |
| SNR (typ) | 89.9 dB | 89.8 dB | 89.0 dB |
| THD (typ) | | | |
| SFDR (typ), incl harm. | -90.4 dB | -90.3 dB | -89.5 dB |
| SINAD (typ) | 86.6 dB | 86.5 dB | 86.0 dB |
| ENOB (based on SINAD) | 14.1 | 14.1 | 14.0 |

Dynamic parameters are measured at ± 1 V input range and 50 Ohm termination with the sample rate specified in the table. Measured parameters are averaged 20 times to get typical values. Test signal is a pure sine wave of the specified frequency with > 99% amplitude. SNR and RMS noise parameters may differ depending on the quality of the used PC. SNR = Signal to Noise Ratio, THD = Total Harmonic Distortion, SFDR = Spurious Free Dynamic Range, SINAD = Signal Noise and Distortion, ENOB = Effective Number of Bits

## Ordering information

| Order No | Description | Order No | Description |
|---|---|---|---|
| UF4520 | UF.4520 with 8 MSample memory and drivers/SBench 5.x | UF4500-16M | 16 MSample onboard memory (total) |
| UF4521 | UF.4521 with 8 MSample memory and drivers/SBench 5.x | UF4500-32M | 32 MSample onboard memory (total) |
| UF4530 | UF.4530 with 8 MSample memory and drivers/SBench 5.x | UF4500-64M | 64 MSample onboard memory (total) |
| UF4531 | UF.4531 with 8 MSample memory and drivers/SBench 5.x | UF4500-128M | 128 MSample onboard memory (total) |
| UF4540 | UF.4540 with 8 MSample memory and drivers/SBench 5.x | UF4500-256M | 256 MSample onboard memory (total) |
| UF4541 | UF.4541 with 8 MSample memory and drivers/SBench 5.x | UF4500-up | Additional handling cost for later memory upgrade |
| UF4500-smod | Star Hub: Synchronisation of 2 - 16 boards, one option per system | UF4500-mr | Multiple Recording: Memory segmentation |
| UF4500.xio | Extra I/O, internal connector: 16 DI/O, 4 Analog out | UF4500-gs | Gated Sampling: Gate signal controls acquisition |
| UF4500-time | Timestamp option: Extra memory for trigger time | UF4500-cs | Synchronisation of 2 - 4 boards, one option per system |
| UF4500-xmf | Extra I/O, external connector: 24 DI/O, 4 Analog out, incl. cable | | |
| Cab-3f-9m-80 | Adapter cable: SMB female to BNC male 80 cm | UF4500-dl | DASYLab driver for UF.4500 series |
| Cab-3f-9m-200 | Adapter cable: SMB female to BNC male 200 cm | UF4500-hp | VEE driver for UF.4500 series |
| Cab-3f-9f-80 | Adapter cable: SMB female to BNC female 80 cm | UF4500-lv | LabVIEW driver for UF.4500 series |
| Cab-3f-9f-200 | Adapter cable: SMB female to BNC female 200 cm | MATLAB | MATLAB driver for all UltraFast boards |

**Technical changes and printing errors are possible**