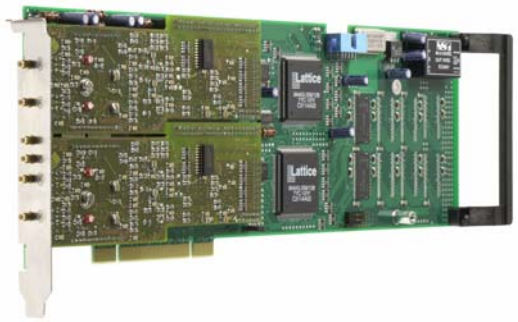
UltraFast

STRATEGIC TEST

UF.2000 - 8 bit transient recorders up to 200 MS/s

- **Standard PCI format**
- **Up to 200 MS/s on two channels**
- **Up to 100 MS/s on four channels**
- **Simultaneously sampling on all channels**
- **7 input ranges: ±50 mV up to ± 5 V**
- **Up to 512 MSample memory**
- **FIFO mode recording up to 100 MB/s to PC**
- **Window and pulsewidth trigger**
- **Input offset up to ±400%**
- **Multi-card synchronization possible**
- **Windows program SBench 5.x included**



Product range overview

All of the UF.2000 series are able to use all of the onboard signal memory, independent of the number of active channels.

Model	1 channel	2 channels	4 channels
UF.2020	50 MS/s	50 MS/s	
UF.2021	50 MS/s	50 MS/s	50 MS/s
UF.2030	200 MS/s	100 MS/s	
UF.2031	200 MS/s	200 MS/s	100 MS/s

Software/Drivers

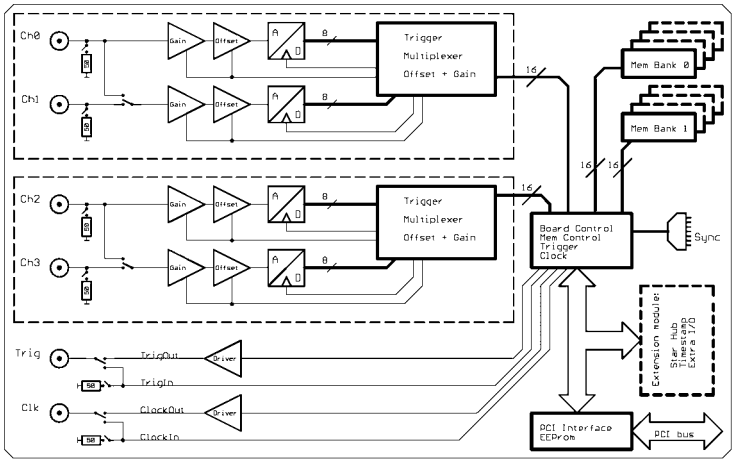
A wide variety of drivers and examples are delivered with the board or are available as an option:

- Windows 98/ME/NT/2000/XP - drivers
- Linux - drivers
- SBench 5.2
- Microsoft Visual C++ examples
- Borland Delphi examples
- Microsoft Visual Basic examples
- Microsoft Excel examples
- LabWindows/CVI examples
- FlexPro support with SBench
- LabVIEW - drivers (as option)
- DASYLab - drivers (as option)
- MATLAB - drivers (as option)
- Agilent VEE - drivers (as option)

General Information

The 4 different UF.2000 PCI boards are designed for fast and high quality data acquisition. Each of the 2 or 4 input channels has it's own 8-bit A/D converter and programmable input amplifier. All channels are recorded simultaneously to eliminate phase delays. Each input can be individually set to one of the seven input ranges by software and can be programmed with an input offset of ±400% of the input range. The extremely large on-board memory allows long time recording even with highest sample rates. The memory can also be used as a FIFO to record data continuously and to process it in the PC or to store it to hard disk.

Hardware block diagram



Software programmable parameters

Sample rate	1 kS/s to max sample rate, external clock, ref clock
Input Range	±50 mV, ±100 mV, ±200 mV, ±500 mV, ±1 V, ±2 V, ±5 V
Input impedance	50 Ohm / 1 MOhm
Input Offset	±400% in steps of 1%
Clock impedance	50 Ohm / 1 MOhm
Trigger impedance	50 Ohm / 1 MOhm
Trigger mode	Channel, External, Software, Auto, Windows, Pulse
Trigger level	1/64 to 63/64 of input range (6 bit)
Trigger edge	rising edge, falling edge or both edges
Trigger pulsewidth	1 to 255 samples in steps of 1 sample
Memory depth	64 up to installed memory in steps of 64
Posttrigger	64 up to 128 M in steps of 64

Application examples

LDA/PDA	Production test	Laboratory equipment
Radar	Spectroscophy	Test of mobile communication
Ultrasound	Medical equipment	

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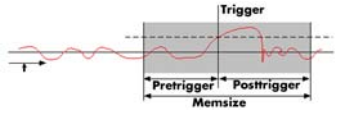
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Possibilities and options

Input impedance

All inputs can be individually switched by software between 50 Ohm and 1 MOhm input impedance. If using fast signals and high sampling rates or you have 50 Ohm cable impedance, then the use of the 50 Ohm termination is recommended to minimise noise and signal reflections. If using weak signal sources or standard probes the use of the 1 MOhm termination is preferred.

Ring buffer mode



The ring buffer mode is the standard mode for all oscilloscope boards. Data is written in a ring memory on the board until a trigger event is detected. After the event the posttrigger values are recorded. Because the data is continuously recorded the pretrigger samples before the event are recorded also : Pretrigger = Memsize - Posttrigger.

FIFO mode

The FIFO mode is designed for continuous data transfer between measurement board and PC memory (up to 100 MB /s) or hard disk (up to 50 MB/s). The data stream is controlled automatically by the driver on interrupt request.

Channel trigger

The data acquisition boards offer a wide variety of trigger modes. In addition to the standard level and edge trigers found on traditional oscilloscopes, it is also possible to define a window trigger where the signal is inside or outside two defined amplitude limits. All trigger modes can be combined with the pulsewidth trigger which is similar to a time window. This is useful for eliminating false triggering due to noise spikes and can also be used to only capture short pulses.

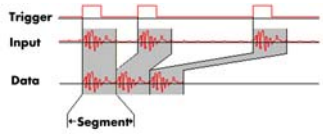
External trigger I/O

All boards include an External Trigger connector for triggering using an external TTL signal. It is possible to use positive or negative edge and this may be combined with a programmable pulsewidth time window trigger. If triggering on a channel or by software, then this trigger event can be output though the external trigger connector to start external instruments.

Pulse width

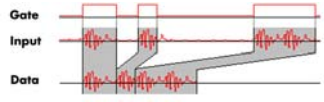
The pulsewidth trigger is similar to a time window. Once the time windows is defined, the pulsewidth trigger is combined with either the channel trigger, pattern trigger and external trigger.It is used to eliminate false triggerring due to noise spikes, but can also be used to capture short events only.

Multiple Recording



The Multiple Recording option is used to record the signals from several trigger events without restarting the hardware. As a result it is possible to record a series of high speed signals, such as RADAR signals where several thousand may need to be captured in a short time. The user defines the number of waveforms to be recorded and the on-board memory is automatically divided in this number of equal-sized segments. Each segment is then filled with data as a trigger event occurs.

Gated Sampling

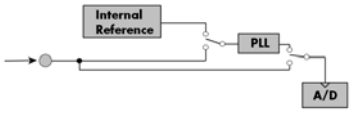


The Gated Sampling option ensures that data is only recorded to memory when the external gate signal reaches a pre-defined level. Effectively, this starts and stops the sampling clock. This option is typically used when you want to reduce the amount of data being recorded to only those signal segments of interest.

External clock I/O

Each UltraFast board is supplied with an External Clock connector. This is used when you want to synchronize the board sampling rate with an external clock signal that may also synchronize other external instruments. It's also possible to output the board generated sampling clock to synchronise external equipment to the board.

Reference clock



This option allows you to use a precise external reference clock (normally 10 MHz) in order to synchronize the board for high-quality measurements with external equipment (like a signal source). It's also possible to enhance the quality of the sampling clock this way. The driver automatically generates the requested sampling clock from the external reference clock signal.

Cascading

The Cascading option is the easiest method to create multi-cards systems. Up to 4 UltraFast boards make be connected. The user is able to define the board that will generate the sampling rate clock which is then fed to the other boards. These other boards can subdivide the sampling rate if required using the onboard hardware divider. Similarly, one board is defined by the user as the trigger master. This board then transmits the trigger signals so that all boards start at the same time. There is a phase delay between two boards of about 500 pico seconds when this synchronisation option is used.

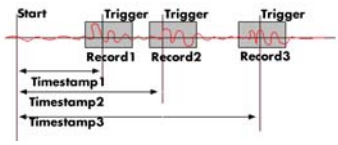
Star Hub

The Star Hub is an additional daughterboard module that allows up to 16 UltraFast boards to be configured as a totally synchronized multi-card system. Unlike the Cascading option, there is no clock or trigger signal phase delay between the boards. The Star Hub module distributes the trigger and clock information between all boards so thatall connected boards are running with the exactly same clock and trigger; athough it is possible to use each boards programmable hardware divider to reduce the sampling rate on different boards.

Extra I/O

The Extra I/O External module adds 24 additional digital I/O lines and 4 analog outputs to the UltraFast board. These additional channels are independent from the high-speed channels and can be controlled asynchronously. An additional PCI backpanel is supplied that houses these additional connectors. There is also an Extra I/O Internal version available with 16 digital I/O and 4 analog output channels. This version is intended for equipment manufacturers who need to route the cables inside the enclosure.

Timestamp



The Timestamp option is used to record the effective time when trigger events occur, into a separate memory buffer. Each timestamp value is derived from the number of samples since the start of the measurement, to a defined zero time or externally synchronised to a radio clock or a GPS receiver. With this option measurements performed on systems at different locations can be synchronized.

Technical Data

Resolution	8 bit	Dimension	312 mm x 107 mm
Differential linearity error (ADC)	0.5 LSB typ.	Width (Standard)	1 full size slot
Integral linearity error (ADC)	0.5 LSB typ.	Width (with star hub option)	2 full size slots
Multi: Trigger to 1st sample delay	fixed	Analogue Connector	3 mm SMB male
Multi: Recovery (re-arm) time	< 20 samples	Overvoltage protection (range < ±500 mV)	±5 V
Trigger accuracy 2/4 channel mode	1 Sample	Overvoltage protection (range > ±500 mV)	±50 V
Trigger accuracy 1 channel mode	2 Samples	Warm up time	10 minutes
Ext. clock: delay to internal clock	42 ns ± 2 ns	Operating temperature	0°C - 50°C
input signal with 50 ? termination	max 5 V rms	Storage temperature	-10°C - 70°C
Trigger output delay	1 Sample	Humidity	10% to 90%
Input impedance	50 Ohm / 1 MOhm || 25 pF		
Min internal clock	1 kS/s	Power consumption 5 V @ full speed	max 3.4 A (17.0 Watt)
Min external clock	1 MS/s	Power consumption 5 V @ power down	max 1.9 A (9.5 Watt)

Input range	±50 mV	±100 mV	±200 mV	±500 mV	±1 V	±2 V	±5 V
Software programmable offset	±200 mV	±400 mV	±800 mV	±2 V	±4 V	±8 V	±20 V
Offset error	< 1 LSB, adjustable by user						
Gain error	< 2 %	< 2 %	< 2 %	< 2 %	< 2 %	< 2 %	< 2 %
UF.202x: Noise (rms): 50 Ohm, 50 MS/s	< 0.5 LSB	< 0.5 LSB	< 0.5 LSB	< 0.5 LSB	< 0.5 LSB	< 0.5 LSB	< 0.5 LSB
UF.203x: Noise (rms): 50 Ohm, 100/200 MS/s	< 2.0 LSB	< 1.5 LSB	< 1.0 LSB	< 1.0 LSB	< 1.0 LSB	< 1.0 LSB	< 1.0 LSB
Crosstalk 5 MHz signal, ±50 mV input, 50 Ohm	< 62 dB						

	UF.2020 UF.2021	UF.2030 UF.2031
max internal clock	50 MS/s	200 MS/s
max external clock	50 MS/s	100 MS/s
-3 dB bandwidth	> 25 MHz	> 90 MHz

Dynamic Parameters

	UF.2020 UF.2021	UF.2030 UF.2031
Test - Sample rate	50 MS/s	100 MS/s
Test signal frequency	1 MHz	1 MHz
SNR (typ)	> 47.5 dB	> 45.9 dB
THD (typ)	< -56.5 dB	< -49.1 dB
SFDR (typ), incl harm.	> 60.0 dB	> 59.5 dB
SINAD (typ)	> 47.0 dB	> 44.2
ENOB (based on SINAD)	7.5	>7.1

Dynamic parameters are measured at ± 1 V input range and 50 Ohm termination with the sample rate specified in the table. Measured parameters are averaged 20 times to get typical values. Test signal is a pure sine wave of the specified frequency with > 99% amplitude. SNR and RMS noise parameters may differ depending on the quality of the used PC. SNR = Signal to Noise Ratio, THD = Total Harmonic Distortion, SFDR = Spurious Free Dynamic Range, SINAD = Signal Noise and Distortion, ENOB = Effective Number of Bits

Ordering information

Order No	Description	Order No	Description
UF2020	UF.2020 with 16 MSample memory and drivers/SBench 5.x	UF2000-32M	32 MSample onboard memory (total)
UF2021	UF.2021 with 16 MSample memory and drivers/SBench 5.x	UF2000-64M	64 MSample onboard memory (total)
UF2030	UF.2030 with 16 MSample memory and drivers/SBench 5.x	UF2000-128M	128 MSample onboard memory (total)
UF2031	UF.2031 with 16 MSample memory and drivers/SBench 5.x	UF2000-256M	256 MSample onboard memory (total)
		UF2000-512M	512 MSample onboard memory (total)
UF2000-smod	Star Hub: Synchronisation of 2 - 16 boards, one option per system	UF2000-up	Additional handling costs for later memory upgrade
UF2000.xio	Extra I/O, internal connector: 16 DI/O, 4 Analog out		
UF2000-xmf	Extra I/O, external connector: 24 DI/O, 4 Analog out, incl. cable	UF2000-mr	Multiple Recording: Memory segmentation
UF2000-time	Timestamp option: Extra memory for trigger time	UF2000-gs	Gated Sampling: Gate signal controls acquisition
		UF2000-cs	Synchronisation of 2 - 4 boards, one option per system
Cab-3f-9m-80	Adapter cable: SMB female to BNC male 80 cm		
Cab-3f-9m-200	Adapter cable: SMB female to BNC male 200 cm	UF2000-dl	DASYLab driver for UF.2000 series
Cab-3f-9f-80	Adapter cable: SMB female to BNC female 80 cm	UF2000-hp	VEE driver for UF.2000 series
Cab-3f-9f-200	Adapter cable: SMB female to BNC female 200 cm	UF2000-lv	LabVIEW driver for UF.2000 series
		MATLAB	MATLAB driver for all UltraFast cards

Technical changes and printing errors are possible