UF2 -3100 : 12 bit A/D Digitizers up to 25 MS/s

- **PCI-X interface (100% compatible to PCI)**
- **Multi channel 12 bit A/D converter board**
- **Versions with 1 MS/s, 10 MS/s and 25 MS/s**
- **2, 4 or 8 channels per card**
- **Simultaneously sampling on all channels**
- **Separate ADC and amplifier per channel**
- **8 input ranges: ±50 mV up to ±10 V**
- **Up to 2 GSample (4 GByte) on-board memory**
- **Sustained streaming mode up to 200 MB/s**
- **Window, pulse width, re-arm, OR/AND trigger**
- **Programmable input offset of ±100%**
- **Multi-card synchronization option for up to 16 cards**
- **Options: synchronous digital channels, ABA mode**



Product range overview

Based on more than 16 years design pedigree, the UltraFast cards are high quality, low-noise instruments that replace traditional oscilloscopes and transient recorders.

Model	1 channel	2 channels	4 channels	8 channels
UF2 -3110	1 MS/s	1 MS/s		
UF2 -3111	1 MS/s	1 MS/s	1 MS/s	
UF2 -3112	1 MS/s	1 MS/s	1 MS/s	1 MS/s
UF2 -3120	10 MS/s	10 MS/s		
UF2 -3121	10 MS/s	10 MS/s	10 MS/s	
UF2 -3122	10 MS/s	10 MS/s	10 MS/s	10 MS/s
UF2 -3130	25 MS/s	25 MS/s		
UF2 -3131	25 MS/s	25 MS/s	25 MS/s	
UF2 -3132	25 MS/s	25 MS/s	25 MS/s	25 MS/s

General Information

The UF2 -3100 series contains nine different cards with a choice of two, four or eight channels and sampling rates of 1 MS/s, 10 MS/s or 25 MS/s; making it possible to choose the most cost-effective solution. As an option 4 digital inputs per channel can be recorded synchronously. With the possibility of up to 2 GSample onboard memory, even the fastest signals can be recorded for long periods. At slower sample rates, the FIFO mode is available for continuous streaming of longer signals to PC RAM or hard disk. Each channel has independent an A/D, voltage range and offset adjustment allowing the user to perfectly match this to each sensor. All channels are simultaneously recorded with no phase errors.

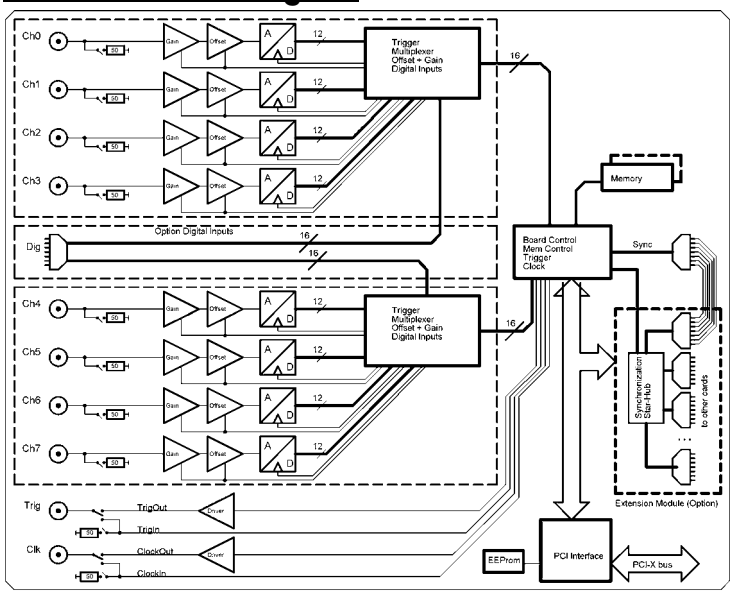
UF2

- Completely new developed base card
- 4 GByte memory with one slot width
- Optimized low jitter clock section
- Multi, Gate with programmable pre, posttrigger and timestamp
- Zero phase delay synchronization
- AND/OR conjunction of trigger/gate

Application examples

Automation	Military	Automotive
Quality control	Production	ATE

Hardware block diagram



Software programmable parameters

Input Range	±50 mV, ±100 mV, ±200 mV, ±500 mV, ±1 V, ±2 V, ±5 V, ±10 V
Input impedance	50 Ohm / 1 MOhm
Input Offset	±100% of input range in steps of 1%
Clock mode	Int. PLL, int. quartz, ext. clock, ext. divided, ext. reference clock, sync
Clock impedance	50 Ohm / high impedance (> 4kOhm)
Trigger impedance	50 Ohm / high impedance (> 4kOhm)
Trigger mode	Channel, Extern, SW, Auto, Window, Pulse, Re-Arm, Or/And, Delay
Trigger level resolution	TBD
Trigger edge	Rising edge, falling edge or both edges
Trigger pulse width	0 to [64k - 1] samples in steps of 1 sample
Trigger delay	0 to [64k - 1] samples in steps of 1 sample
Memory depth	8 up to [installed memory / number of active channels] in steps of 4
Posttrigger	4 up to [8G - 4] samples in steps of 4
Multiple Recording segment size	8 up to[installed memory / 2 / active channels] in steps of 4
Multi / Gated pretrigger	0 up to [8k samples / number of active channels - 16]
ABA clock divider	1 up to [64k - 1] in steps of 1
Synchronization clock divider	2 up to [8k - 2] in steps of 2
Channel selection	Any number of available channels (see manual for selection limits)

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Software Support

Windows drivers

The cards are delivered with drivers for Windows XP, Windows XP64, Windows Visa (Beta) and Windows XP64. Programming examples for Visual C/C++, Borland C++ Builder, Gnu C, LabWindows/CVI, Borland Delphi and Visual Basic are included.

Linux Drivers



All cards are delivered with full Linux support. Pre compiled kernel modules are included for the most common distributions like RedHat, Suse or Debian. The Linux support is enhanced by SMP support, versatile programming examples as well as the possibility to obtain the driver sources for compilation on your own PC.

SBench

A full licence of SBench, the easy-to-use measurement and signal generation program for the UltraFast cards, is included in the delivery. Version 6 is running under Windows as well as under Linux (KDE and GNOME)

Third-party products

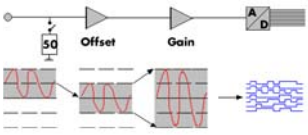
We offer the widest third-party products support. Optional drivers are available for LabVIEW, MATLAB, DASYLab and Agilent VEE. All drivers come with examples and detailed documentation.

UF Software compatibility layer

To allow easy migration from UF cards to the new UF2 cards for existing software, a special software compatibility layer is delivered with the cards. This DLL converts UF calls to UF2 calls and simulates a UF card in the software.

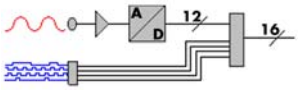
Hardware features and options

Input Amplifier



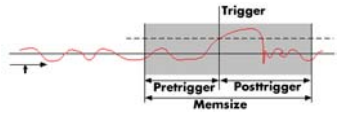
The analog inputs can be adapted to real world signals using a wide variety of settings that are independent for each channel. By using software commands the input termination can be changed to 50 Ohm or 1 MOhm, the matching input range can be selected and the signal offset can be adjusted.

Digital inputs



This option acquires additional synchronous digital channels phase-stable with the analog data. When the option is installed there are 4 additional digital inputs for every analog A/D channel.

Standard mode



The Standard mode allows the Digitizer card to sample at it's maximum rates and running independently of the host PC so that it's cpu can be used for other tasks. Data is written in a ring buffer on the board until a trigger event is detected. After this event the posttrigger values are recorded. The samples prior to the trigger event are also visible: Pretrigger = Memsize - Posttrigger. After the last sample of the measurement has been recorded, the data can then be transferred to the host PC memory (not before)

FIFO mode

The FIFO mode is designed for continuous data transfer between measurement board and PC memory, so that signals longer than the available card memory can be recorded directly to the PC. The maximum sampling rate is limited by the speed that data can be continuously offloaded from the card to the PC and stored. On a PCI-X slot (64 MHz/32-bit PCI bus) this is 200 MB/s, and up to 100 MB/s on a traditional PCI (33 MHz/32-bit) slot. The control of the data stream is automatically managed by the driver on interrupt request.

All installed on-board memory is used for buffer data, making the continuous streaming extremely reliable. The standard memory supplied on the card is sufficient for reliable operation.

Channel trigger

The Digitizer boards provide a wide variety of trigger modes. Apart from the standard level and edge trigger found on traditional oscilloscopes, it is also possible to define a window trigger. All trigger modes can be combined with the pulsewidth trigger that makes it possible to trigger on signal errors, such as too long or too short pulses by defining a time-window when the event should/should not occur. There is also a re-arming mode for accurate trigger recognition on noisy signals. Finally, the card can be configured with a AND/OR combination of different trigger events. A unique feature of these cards is the possibility to select deactivated channels as trigger sources.

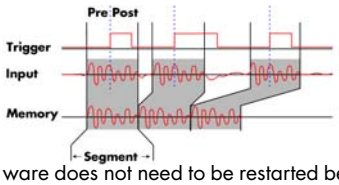
External trigger I/O

All boards can be triggered using an external TTL signal. It is possible to use positive or negative edge in combination with a programmable pulse width. An internally recognised trigger event can, when activated by software, be routed to the trigger connector to start external instruments.

Pulse width

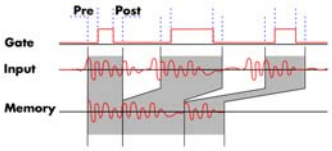
Defines the minimum or maximum width that a trigger pulse must have to generate a trigger event. Can be combined with channel trigger, pattern trigger and external trigger.

Multiple Recording



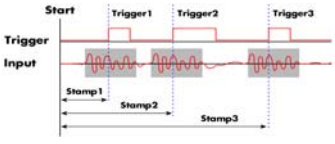
The Multiple Recording option is used to record a high-speed series of waveforms, each with a unique trigger event and an extremely short re-arming time. The hardware does not need to be restarted between triggers. The on-board memory is divided in segments of the same size. Each of them is filled with data if a trigger event occurs. Pre- and posttrigger of the segments can be programmed. The number of acquired segments is only limited by the used memory and is unlimited when using FIFO mode. A typical application is to record RADAR pulses.

Gated Sampling



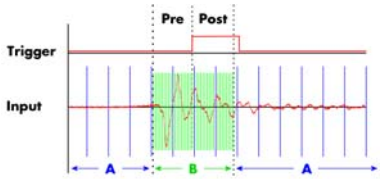
The Gated Sampling option allows data recording controlled by an external gate signal. Data is only recorded if the gate signal has reached a programmed level. In addition, a pre-segment before start of the gate signal as well as a post segment after end of gate signal can be acquired. The number of gate segments is only limited by the used memory and is unlimited when using FIFO mode.

Timestamp



The timestamp option writes the time positions of the trigger events in an extra memory. The timestamps are relative to the start of the recording, a defined zero time, externally synchronised to a radio clock, or a GPS receiver. With this option acquisitions of systems on different locations can be set in a precise time relation.

ABA mode



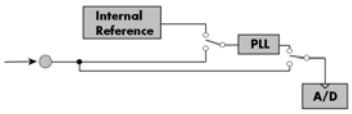
The optional ABA mode combines slow continuous data recording with fast acquisition on trigger events. The ABA mode works like a slow data logger combined

with a fast digitizer. The exact position of the trigger events is stored as timestamps in an extra memory.

External clock I/O

Using a dedicated connector a sampling clock can be fed in from an external system. It is also possible to output the internally used sampling clock to synchronise external equipment to this clock.

Reference clock



The option to use a precise external reference clock (normally 10 MHz) is necessary to synchronise the board for high-quality measurements with external equipment (like a signal source). It is also possible to enhance the quality of the sampling clock in this way. The driver automatically generates the requested sampling clock from the fed in reference clock.

Star-Hub



The Star Hub is an additional module allowing phase stable synchronisation of up to 16 boards. There is no phase delay between any channels, independently of the number of boards. The Star Hub distributes trigger and clock information between all boards. As a result, all connected boards are running with the same clock and the same trigger. All trigger sources can be combined with OR/AND allowing all channels of all cards to be the trigger source. The Star Hub is available as a 5 card or a 16 card version. The 5 card version does not need an extra PCI slot width.

Technical Data

Analog Inputs

Resolution	12 bit
Differential non linearity (DNL)	≤ 1 LSB (ADC)
Integral non linearity (INL)	≤ 2.5 LSB (ADC)
Offset error	can be calibrated by user
Gain error	< 1% of current value
Programmable input offset	±100% of current input range
Crosstalk: ±50 mV, 50 Ohm, 500 kHz	< -70 dB between any adjacent channels
Input signal with 50 Ohm termination	max 5 V rms
Analog Input impedance	50 Ohm / 1 MOhm || 25 pF
Over voltage protection (range ≤ ±1 V)	±5 V
Over voltage protection (range > ±1 V)	±50 V
Connector (analog and trigger/clock)	3 mm SMB male

Trigger

Multi, Gate: re-arming time	<4 Samples
Max Pretrigger at Multi, Gate, FIFO	8176 Samples as sum of all active channels
Internal/External trigger accuracy	1 Sample
Channel trigger resolution	TBD
Trigger output delay	TBD
External trigger type	TTL compatible
External trigger input	Low ≤ 0.8 V, High ≥ 2.0 V, ≥ 2 clock periods
External trigger maximum voltage	-0.5 V up to +5.5 V
External trigger output levels	Low ≤ 0.4 V, High ≥ 2.4 V, TTL compatible
External trigger output drive strength	Capable of driving 50 ohm load

Power consumption (max speed)	3,3 V	TBD	0.0 A	0.0 A
UF2 -31x0	TBD	TBD	0.0 A	0.0 A
UF2 -31x1	TBD	TBD	0.0 A	0.0 A
UF2 -31x2	TBD			

Certifications and Compliances

EMC Immunity	Compliant with CE Mark
EMC Emission	Compliant with CE Mark

Clock

Internal clock range (PLL mode)	1 kS/s to max (see table below)
Internal clock accuracy	20 ppm
Internal clock: max. jitter in PLL mode	TBD
Internal clock: max. jitter in quartz mode	TBD
Internal clock setup granularity	≤1% of range (100M, 10M, 1M, 100k,...
Internal clock setup granularity example	range 1M to 10M: stepsize ≤ 100k
Reference clock: external clock range	≥ 4.0 MHz and ≤ 125.0 MHz
External clock range	1 kS/s to max (see table below)
External clock delay to internal clock	TBD
External clock input	Low ≤ 0.8 V, High ≥ 2.0 V, duty 45% - 55%
External clock maximum voltage	-0.5 V up to +5.5 V
External clock output levels	Low ≤ 0.4 V, High ≥ 2.4 V, TTL compatible
External clock output drive strength	Capable of driving 50 ohm load

Digital inputs: input impedance	110 Ohm @ 2.5V
Digital inputs delay to analog sample	TBD
Maximum voltage	-0.3 V up to +5.5 V
Input voltage	Low ≤ 0.8 V, High ≥ 2.0 V
Connector (digital inputs)	40 pole half pitch (Hirose FX2 series)

Environmental and Physical details

Dimension (PCB only)	312 mm x 107 mm (full PCI length)
Width (Standard or star-hub 5)	1 full size slot
Width (star-hub 16)	2 full size slots
Width (with digital inputs)	1 full size slots + 1 half size slot
Weight (depending on options/channels)	290g (2/4 ch) up to 460g (8 ch + dig + sh)
PCI / PCI-X bus slot compatibility	32 bit or 64 bit, 33 MHz up to 133 MHz
Warm up time	10 minutes
Operating temperature	0°C - 50°C
Storage temperature	-10°C - 70°C
Humidity	10% to 90%

Dynamic Parameters

	UF2 -3110 UF2 -3111		UF2 -3112		UF2 -3120 UF2 -3121		UF2 -3122		UF2 -3130 UF2 -3131		UF2 -3132	
max internal clock	1 MS/s		1 MS/s		10 MS/s		10 MS/s		25 MS/s		25 MS/s	
max external clock	1 MS/s		1 MS/s		10 MS/s		10 MS/s		25 MS/s		25 MS/s	
-3 dB bandwidth	DC to 500 kHz		DC to 500 kHz		DC to 5 MHz		DC to 5 MHz		DC to 12.5 MHz		DC to 12.5 MHz	
Zero noise level (range ≤ ±100 mV)	TBD		TBD		TBD		TBD		TBD		TBD	
Zero noise level (range > ±100 mV)	TBD		TBD		TBD		TBD		TBD		TBD	
Test - sampling rate	1 MS/s		1 MS/s		10 MS/s		10 MS/s		25 MS/s		25 MS/s	
Test signal frequency	10 kHz	90 kHz	10 kHz	90 kHz	90 kHz	1 MHz	90 kHz	1 MHz	1 MHz	4 MHz	1 MHz	4 MHz
SNR (typ)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
THD (typ)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
SFDR (typ), excl. harm.	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
ENOB (based on SINAD)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Dynamic parameters are measured at ± 1 V input range (if no other range is stated) and 50 Ohm termination with the samplerate specified in the table. Measured parameters are averaged 20 times to get typical values. Test signal is a pure sine wave of the specified frequency with > 99% amplitude. SNR and RMS noise parameters may differ depending on the quality of the used PC. SNR = Signal to Noise Ratio, THD = Total Harmonic Distortion, SFDR = Spurious Free Dynamic Range, SINAD = Signal Noise and Distortion, ENOB = Effective Number of Bits. For a detailed description please see application note 002.

Ordering Information

Versions

Order no.	1 channel	2 channels	4 channels	8 channels
UF2 -3110	1 MS/s	1 MS/s		
UF2 -3111	1 MS/s	1 MS/s	1 MS/s	
UF2 -3112	1 MS/s	1 MS/s	1 MS/s	1 MS/s
UF2 -3120	10 MS/s	10 MS/s		
UF2 -3121	10 MS/s	10 MS/s	10 MS/s	
UF2 -3122	10 MS/s	10 MS/s	10 MS/s	10 MS/s
UF2 -3130	25 MS/s	25 MS/s		
UF2 -3131	25 MS/s	25 MS/s	25 MS/s	
UF2 -3132	25 MS/s	25 MS/s	25 MS/s	25 MS/s

Memory

Order no.	Option
UF2 -3100-64MS	Memory upgrade to 64 MSample (128 MB) total memory
UF2 -3100-128MS	Memory upgrade to 128 MSample (256 MB) total memory
UF2 -3100-256MS	Memory upgrade to 256 MSample (512 MB) total memory
UF2 -3100-512MS	Memory upgrade to 512 MSample (1 GB) total memory
UF2 -3100-1GS	Memory upgrade to 1 GSample (2 GB) total memory
UF2 -3100-2GS	Memory upgrade to 2 GSample (4 GB) total memory

Options

Order no.	Option
UF2 -3100-mr	Option Multiple Recording
UF2 -3100-mgt	Option pack including Multiple Recording, Gated Sampling, Timestamp
UF2 -3100-mgtab	Option pack including Multiple Recording, Gated Sampling, Timestamp, ABA mode
UF2 -3100-SH5 (1)	Synchronization Star-Hub for up to 5 cards, only 1 slot width
UF2 -3100-SH16 (1)	Synchronization Star-Hub for up to 16 cards
UF2 -3100-dig	Additional synchronous digital inputs (4 per analog channel) including Cab-d40-idc-100
UF2 -3100-bxio	Option BaseXIO: 8 digital I/O lines usable as asynchronous I/O, timestamp ref-clock and additional external trigger lines, additional bracket with 8 SMB connectors

Cables

Order no.	Option
Cab-3f-9m-80	Adapter cable SMB female to BNC male, 80 cm
Cab-3f-9f-80	Adapter cable SMB female to BNC female, 80 cm
Cab-3f-3f-80	Adapter cable SMB female to SMB female, 80 cm
Cab-3f-9m-200	Adapter cable SMB female to BNC male, 200 cm
Cab-3f-9f-200	Adapter cable SMB female to BNC female, 200 cm
Cab-3f-3f-200	Adapter cable SMB female to SMB female, 200 cm
Cab-3f-9f-5	Adapter cable SMB female to BNC female, 5 cm (short cable especially for oscilloscopes probes)
Cab-d40-idc-100	Flat ribbon cable 40 pole FX2 for digital connector to 2x20 pole IDC connector, 100 cm
Cab-d40-d40-100	Flat ribbon cable 40 pole FX2 for digital connector to 40 pole digital FX2 connector, 100 cm

Drivers

Order no.	Option
UF2 -ml	MATLAB driver for all UF2 cards
UF2 -3100-lv	LabVIEW driver for all UF2 -3100 cards
UF2 -3100-dl	DASYLab driver for all UF2 -3100 cards
UF2 -3100-vee	Agilent VEE driver for all UF2 -3100 cards

technical changes and printing errors possible

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