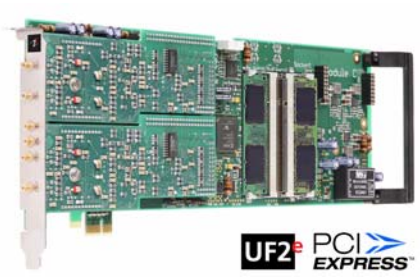
UF2e-2000 : 8 bit Waveform Digitizers / Transient Recorders up to 200 MS/s

- **PCI Express x1 boards for PC's**
- **Up to 200 MS/s on 2 channels, 100 MS/s on 4 channels**
- **Simultaneously sampling on all channels**
- **Separate ADC and amplifier per channel**
- **7 input ranges: ±50 mV up to ± 5 V**
- **Up to 4 GSample on-board memory**
- **64 MS standard memory installed**
- **Every board has up to 150 MB/s data transfer to PC**
- **Window, pulse width, re-arm, OR/AND trigger**
- **Programmable input offset of ±400%**
- **Synchronization of up to 16 cards per system and up to 271 cards with system sync**
- **ABA mode option: combination of data logger and fast digitizer on trigger**
- **Versatile software support for Windows and Linux**



Product range overview

PCI Express is the latest bus for PC-based accessory cards and seen as the replacement to 33/66 MHz PCI. Compared to the old PCI bus, PCI Express x1 has the advantage that every card has a maximum continous transfer rate of 150 MBytes/s. With PCI the bus bandwidth is shared by all cards.

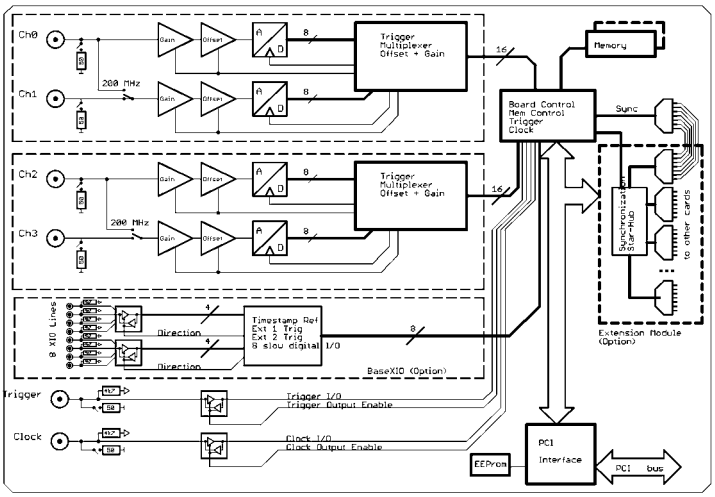
Model	1 channel	2 channels	4 channels
UF2e-2020	50 MS/s	50 MS/s	
UF2e-2021	50 MS/s	50 MS/s	50 MS/s
UF2e-2030	200 MS/s	100 MS/s	
UF2e-2031	200 MS/s	200 MS/s	100 MS/s

General Information

The UF2e-2000 series are designed for the fast and high quality data acquisition. Each channel has it's own 100 MS/s or 50 MS/s ADC for true simultaneous sampling and input amplifer that allows the user match the input range to the signal to optimize the full scale range and A/D resolution. Auto-calibration removes dcV offset errors and input impedance of 50 Ohm or 1 MOhm can be selected.
Like all our boards, the UF2e-2000 series supports recording to card memory with off-load at the end of the measurement for recording on all channels at max samping rate, or continuous streaming to the host PC RAM or hard disks with DMA scatter-gather to record signals for hours (PCI bus bandwidth and disk speed permitting).

UF2e
- Completely new developed base card
- 4 GByte memory with one slot width
- Optimized low jitter clock section
- Multi, Gate with programmable pre, posttrigger and timestamp
- Zero phase delay synchronization
- AND/OR conjunction of trigger/gate

Hardware block diagram



Software programmable parameters

Input Range	±50 mV, ±100 mV, ±200 mV, ±500 mV, ±1 V, ±2 V, ±5 V
Input impedance	50 Ohm / 1 MOhm
Input Offset	±400% of input range in steps of 1%
Clock mode	Int. PLL, int. quartz, ext. clock, ext. divided, ext. reference clock, sync
Clock impedance	50 Ohm / high impedance (> 4kOhm)
Trigger impedance	50 Ohm / high impedance (> 4kOhm)
Trigger mode	Channel, Extern, SW, Auto, Window, Pulse, Re-Arm, Or/And, Delay
Trigger level	8 bit resolution: 1/256 to 255/256 of input range
Trigger edge	Rising edge, falling edge or both edges
Trigger pulse width	0 to [64k - 1] samples in steps of 1 sample
Trigger delay	0 to [64k - 1] samples in steps of 1 sample
Memory depth	8 up to [installed memory / number of active channels] in steps of 8
Posttrigger	4 up to [8G - 4] samples in steps of 4
Multiple Recording segment size	8 up to[installed memory / 2 / active channels] in steps of 4
Multi / Gated pretrigger	0 up to [16k samples / number of active channels - 32]
ABA clock divider	1 up to [64k - 1] in steps of 1
Synchronization clock divider	2 up to [8k - 2] in steps of 2
Channel selection	Any 1, 2 or 4 channels (see manual for clock limits on the selections)

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Software Support

Windows drivers

The cards are delivered with drivers for Windows 2000, Windows XP, Windows XP64 and Windows Vista. Programming examples for Visual C/C++, Borland C++ Builder, LabWindows/CVI, Borland Delphi, Visual Basic and VB.NET are included.

Linux Drivers

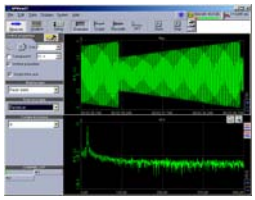


All cards are delivered with full Linux support. Pre compiled kernel modules are included for the most common distributions like RedHat, Fedora, Suse or Debian. The Linux support includes SMP systems, 32 bit and 64 bit systems, versatile programming examples for Gnu C++ as well as the possibility to get the driver sources for own compilation.

SBench

The UF2e cards come with a full licence of the SBench program for measurement, analysis and reports. Version 6 is runs under Windows as well as under Linux (KDE and GNOME).

SPViewIT



SPviewIT is the professional streaming software solution that is optimised for continuous data acquisition of large amounts of data. Key features of SPviewIT are different data displays, editable interface and a large number of export filters. A demo version comes with the card.

Third-party products

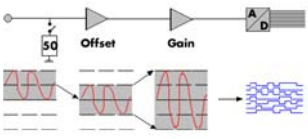
Drivers are available as a cost-option for LabVIEW, MATLAB, DASYLab and Agilent VEE. All drivers come with examples and detailed documentation.

UF Software compatibility layer

For existing customers of the UF cards, a special software compatibility layer is delivered with the UF2e cards. This DLL converts UF calls to UF2e calls and simulates a UF card in the software.

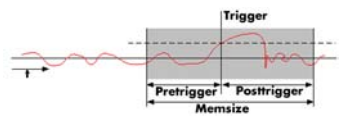
Hardware features and options

Input Amplifier



The analog inputs can be adapted to real world signals using a wide variety of settings that are individual for each channel. By using software commands the input termination can be changed between 50 Ohm and 1 MOhm, one can select a matching input range and the signal offset can be compensated for.

Ring buffer mode



The ring buffer mode is the standard mode of all oscilloscope boards. Data is written in a ring memory of the board until a trigger event is detected. After the event the posttrigger values are recorded. This allows the user to record samples prior to the trigger event: Pretrigger = Memsize - Posttrigger.

FIFO mode

The FIFO mode is designed for continuous data transfer between measurement board and PC memory (up to 150 MB/s on a PCI Express x1 slot) or hard disk. The control of the data stream is done automatically by the driver on interrupt request. The complete installed on-board memory is used for buffer data, making the continuous streaming extremely reliable.

Channel trigger

The UF2e boards offer a wide variety of trigger modes. In addition to the standard level and edge found on oscilloscopes it's also possible to define a window trigger. All trigger modes can also be combined with the pulsewidth trigger. This makes it possible to trigger on signal errors like too long or too short pulses. A new re-arming mode is provided for accurate trigger recognition on noisy signals and different triggers can be combined using AND/OR. A unique feature is that it is possible to use deactivated channels as trigger sources.

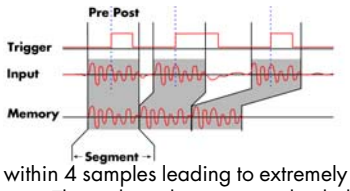
External trigger I/O

All boards can be triggered using an external TTL signal. It's possible to use positive or negative edge also in combination with a programmable pulse width. An internally recognised trigger event can - when activated by software - be routed to the trigger connector to start external instruments.

Pulse width

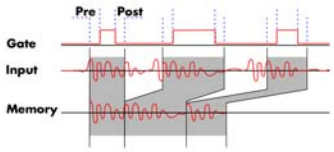
Defines the minimum or maximum width that a trigger pulse must have to generate a trigger event. Pulse width can be combined with channel trigger, pattern trigger and external trigger.

Multiple Recording



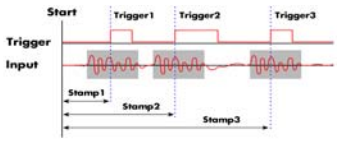
The Multiple Recording option allows recording of high-speed trigger events with an extremely short re-arming time e.g. RADAR signals. The trigger re-arming is achieved within 4 samples leading to extremely fast Pulse Repetition Frequencies. The on-board memory is divided in several segments of the same size, each being filled with data as a trigger event occurs. Pre- and posttrigger of the segments can be programmed. The number of acquired segments is only limited by the used memory and is unlimited when using the FIFO mode.

Gated Sampling



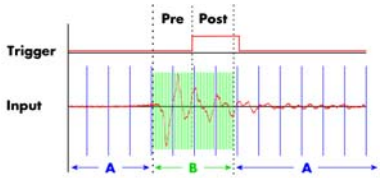
The Gated Sampling option allows data recording controlled by an external gate signal. Data is only recorded if the gate signal has a programmed level. In addition a pre-area before start of the gate signal as well as a post area after end of the gate signal can be acquired. The number of gate segments is only limited by the used memory and is unlimited when using FIFO mode.

Timestamp



The timestamp option writes the time positions of the trigger events in an extra memory. The timestamps are relative to the start of recording, a defined zero time, externally synchronised to a radio clock, or a GPS receiver. With this option acquisitions of systems on different locations can be set in a precise time relation.

ABA mode

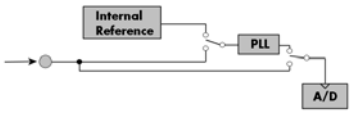


The optional ABA mode combines slow continuous data recording with fast acquisition on trigger events. The ABA mode works like a slow data logger combined with a fast digitizer. The exact position of the trigger events is stored as timestamps in an extra memory.

External clock I/O

Using a dedicated connector a sampling clock can be fed in from an external system. It's also possible to output the internally used sampling clock to synchronise external equipment to this clock.

Reference clock



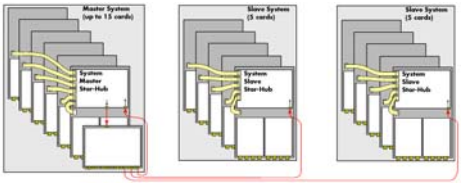
The option to use a precise external reference clock (normally 10 MHz) is necessary to synchronise the board for high-quality measurements with external equipment (like a signal source). It's also possible to enhance the quality of the sampling clock in this way. The driver automatically generates the requested sampling clock from the fed in reference clock.

Star Hub



The Star Hub is an additional module allowing the phase stable synchronisation of up to 16 boards in one system. Independent of the number of boards there is no phase delay between all channels. The Star Hub distributes trigger and clock information between all boards and as a result all connected boards are running with the same clock and the same trigger. All trigger sources can be combined with OR/AND allowing all channels of all cards to be trigger source at the same time. The Star Hub is available as 5 card and 16 card version (which requires extra PCI slot width).

271 synchronous cards with theSystem Star-Hub



With the help of multiple System Star Hubs it is possible to link up to 17 systems phase synchronous with each other. Each PC can then contain up to 16 cards (master only 15). In total 271 cards can be synchronized. One master system distributes clock and trigger signal to all slave systems.

BaseXIO (enhanced trigger)



The BaseXIO option offers 8 asynchronous digital I/O lines on the base card. The direction can be selected by software in groups of four. Two of these lines can also be used as additional external trigger sources. This allows the building of complex trigger conjunctions with external gated triggers as well as AND/OR conjunction of multiple external trigger sources like, for example, the picture and row synchronisation of video signals. In addition one of the I/O lines can be used as reference clock for the Timestamp counter.

Technical Data

Analog Inputs	
Resolution	8 bit
Differential non linearity (DNL)	≤ 0.5 LSB (ADC)
Integral non linearity (INL)	≤ 0.5 LSB (ADC)
Offset error	can be calibrated by user
Gain error	< 2% of current value
Programmable input offset	±400% of current input range
Crosstalk 1 MHz signal, 50 Ohm term	< -62 dB between any adjacent channels
Input signal with 50 Ohm termination	max 5 V rms
Analog Input impedance	50 Ohm / 1 MOhm || 25 pF
Over voltage protection (range ≤ ±0.5 V)	±5 V
Over voltage protection (range > ±0.5 V)	±50 V
Connector (analog and trigger/clock)	3 mm SMB male

Trigger	
Multi, Gate: re-arming time	<4 Samples
Max Pretrigger at Multi, Gate, FIFO	16352 Samples as sum of all active channels
Trigger accuracy (≤100 MS/s)	1 Sample (internal or external trigger mode)
Trigger accuracy (>100 MS/s)	2 Samples (internal or external trigger mode)
Channel trigger resolution	8 bit
Trigger output delay	One positive edge after internal trigger event
External trigger type	3.3V LVTTL compatible (5V tolerant)
External trigger input	Low ≤ 0.8 V, High ≥ 2.0 V, ≥ 2 clock periods
External trigger maximum voltage	-0.5 V up to +4.0 V (internally clamped to 3.3V, 100 mA max. clamping current)
External trigger output levels	Low ≤ 0.4 V, High ≥ 2.4 V, TTL compatible
External trigger output drive strength	Capable of driving 50 ohm load

BaseXIO (Option)	
BaseXIO Connector (extra bracket)	8 x SMB (8 x MMCX internal)
BaseXIO input	TTL compatible: Low ≤ 0.8 V, High ≥ 2.0 V
BaseXIO input maximum voltage	-0.5 V up to +5.5 V
BaseXIO output levels	TTL compatible: Low ≤ 0.4 V, High ≥ 2.4 V
BaseXIO output drive strength	32 mA maximum current

Certifications and Compliances	
EMC Immunity	Compliant with CE Mark
EMC Emission	Compliant with CE Mark

Clock	
Internal clock range (PLL mode)	1 kS/s to max (see table below)
Internal clock accuracy	20 ppm
Internal clock: max. jitter in PLL mode	TBD
Internal clock: max. jitter in quartz mode	TBD
Internal clock setup granularity	≤1% of range (100M, 10M, 1M, 100k,...)
Internal clock setup granularity example	range 1M to 10M: stepsize ≤ 100k
Reference clock: external clock range	≥ 4.0 MHz and ≤ 125.0 MHz
External clock range	1 MS/s to max (see table below)
External clock delay to internal clock	5.4 ns
External clock type	3.3V LVTTL compatible
External clock input	Low ≤ 0.8 V, High ≥ 2.0 V, duty 45% - 55%
External clock maximum voltage	-0.5 V up to +3.8 V (internally clamped to 3.3V, 100 mA max. clamping current)
External clock output levels	Low ≤ 0.4 V, High ≥ 2.4 V, TTL compatible
External clock output drive strength	Capable of driving 50 ohm load

Environmental and Physical details	
Dimension (PCB only)	312 mm x 107 mm (full PCI length)
Width (Standard or star-hub 5)	1 full size slot
Width (star-hub 16)	2 full size slots
Weight (depending on options/channels)	290g (2 ch) up to 420g (4 ch + sh)
PCI Express slot type	x1
PCI Express compatibility	any type of PCI Express slot
Warm up time	10 minutes
Operating temperature	0°C - 50°C
Storage temperature	-10°C - 70°C
Humidity	10% to 90%

Power consumption (max speed)	**3.3 V**	**5 V**	**-12 V**	**+12V**	**Total**
UF2e-20x0 (64 MS memory)	2.2 A	0.5 A	n.u.	n.u.	9.8 W
UF2e-20x1 (64 MS memory)	2.8 A	0.8 A	n.u.	n.u.	13.3 W
UF2e-2031 (4 GS memory), max power	3.9 A	0.8 A	n.u.	n.u.	16.9 W

Max channels / Star-Hub Option	**SH5**	**SH16**	**SSHS5**	**SSHS16**
UF2e-2020/2030	10	32	170	542
UF2e-2021/2031	20	64	340	1084

Dynamic Parameters

	UF2e-2020		UF2e-2021		UF2e-2030		UF2e-2031	
max internal clock	50 MS/s		50 MS/s		200 MS/s		200 MS/s	
max external clock	50 MS/s		50 MS/s		100 MS/s		100 MS/s	
-3 dB bandwidth	DC to 25 MHz		DC to 25 MHz		DC to 90 MHz		DC to 90 MHz	
Zero noise level (≤ ±100 mV)	≤ 0.6 LSB		≤ 0.9 LSB		≤ 1.5 LSB		≤ 2.0 LSB	
Zero noise level (> ±100 mV)	≤ 0.6 LSB		≤ 0.7 LSB		≤ 1.3 LSB		≤ 1.5 LSB	
Test - sampling rate	50 MS/s		50 MS/s		100 MS/s		100 MS/s	
Test signal frequency	1 MHz	4 MHz	1 MHz	4 MHz	1 MHz	9 MHz	1 MHz	9 MHz
SNR (typ)	47.5 dB	47.5 dB	46.8 dB	46.5 dB	45.3 dB	45.0 dB	45.0 dB	44.5 dB
THD (typ)	-56.0 dB	-55.5 dB	-56.0 dB	-55.5 dB	-51.5 dB	-49.5 dB	-49.5 dB	-49.5 dB
SFDR (typ), excl. harm.	61.3 dB	61.0 dB	60.3 dB	60.1 dB	59.0 dB	57.0 dB	59.0 dB	57.0 dB
ENOB (based on SNR)	7.6 bit	7.6 bit	7.5 bit	7.4 bit	7.2 bit	7.2 bit	7.2 bit	7.2 bit
ENOB (based on SINAD)	7.5 bit	7.5 bit	7.4 bit	7.3 bit	7.1 bit	7.0 bit	7.1 bit	7.0 bit

Dynamic parameters are measured at ± 1 V input range (if no other range is stated) and 50 Ohm termination with the samplerate specified in the table. Measured parameters are averaged 20 times to get typical values. Test signal is a pure sine wave of the specified frequency with > 99% amplitude. SNR and RMS noise parameters may differ depending on the quality of the used PC. SNR = Signal to Noise Ratio, THD = Total Harmonic Distortion, SFDR = Spurious Free Dynamic Range, SINAD = Signal Noise and Distortion, ENOB = Effective Number of Bits. For a detailed description please see application note 002.

Order Information

Versions

Order no.	Standard mem	1 channel	2 channels	4 channels
UF2e-2020	64 MByte	50 MS/s	50 MS/s	
UF2e-2021	64 MByte	50 MS/s	50 MS/s	50 MS/s
UF2e-2030	64 MByte	200 MS/s	100 MS/s	
UF2e-2031	64 MByte	200 MS/s	200 MS/s	100 MS/s

Memory

Order no.	Option
UF2e-2000-128MB	Memory upgrade to 128 MB of total memory
UF2e-2000-256MB	Memory upgrade to 256 MB of total memory
UF2e-2000-512MB	Memory upgrade to 512 MB of total memory
UF2e-2000-1GB	Memory upgrade to 1 GB of total memory
UF2e-2000-2GB	Memory upgrade to 2 GB of total memory
UF2e-2000-4GB	Memory upgrade to 4 GB of total memory

Options

Order no.	Option
UF2e-2000-mr	Option Multiple Recording
UF2e-2000-mgt	Option pack including Multiple Recording, Gated Sampling, Timestamp
UF2e-2000-mgtab	Option pack including Multiple Recording, Gated Sampling, Timestamp, ABA mode
UF2e-2000-SH5 (1)	Synchronization Star-Hub for up to 5 cards, only 1 slot width
UF2e-2000-SH16 (1)	Synchronization Star-Hub for up to 16 cards
UF2e-2000-SSHM (1)	System-Star-Hub Master for up to 15 cards in the system and up to 17 systems, sync cables included
UF2e-2000-SSHS5 (1)	System-Star-Hub Slave for up to 5 cards in one system, all sync cables included
UF2e-2000-SSHS16 (1)	System-Star-Hub Slave for up to 16 cards in one system, all sync cables included
UF2e-2000-bxio	Option BaseXIO: 8 digital I/O lines usable as asynchronous I/O, timestamp ref-clock and additional external trigger lines, additional bracket with 8 SMB connectors
UF2e-upgrade	Upgrade for UF2e-2000: later installation of option -dig or -bxio

Cables

Order no.	Option
Cab-3f-9m-80	Adapter cable SMB female to BNC male, 80 cm
Cab-3f-9f-80	Adapter cable SMB female to BNC female, 80 cm
Cab-3f-3f-80	Adapter cable SMB female to SMB female, 80 cm
Cab-3f-9m-200	Adapter cable SMB female to BNC male, 200 cm
Cab-3f-9f-200	Adapter cable SMB female to BNC female, 200 cm
Cab-3f-3f-200	Adapter cable SMB female to SMB female, 200 cm
Cab-3f-9f-5	Adapter cable SMB female to BNC female, 5 cm (short cable especially for oscilloscope probes)

Drivers

Order no.	Option
UF2e-ml	MATLAB driver for all UF2e cards
UF2e-2000-lv	LabVIEW driver for all UF2e-2000 cards
UF2e-2000-dl	DASYLab driver for all UF2e-2000 cards
UF2e-2000-vee	Agilent VEE driver for all UF2e-2000 cards

(1) : Only one of the options can be installed on a card at a time.

Warranty and Software Maintenance

All UltraFast boards are supplied with a two-year hardware warranty and include life-time technical support and free software updates, including SDK's for future Microsoft Windows and Linux versions.

technical changes and printing errors possible

document: UF2e-20_Datasheet.fm
version: 20070711

STRATEGIC TEST
The High-Speed Specialists

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