SPECTRUM
SYSTEMENTWICKLUNG MICROELECTRONIC GMBH

# MX.30xx - 12 bit transient recorder up to 100 MS/s

- **PXI 3U / CompactPCI 3U format**
- **Fastest 12 bit PXI A/D converter board**
- **Up to 100 MS/s on one channel**
- **Up to 60 MS/s on two channels**
- **Simultaneously sampling on all channels**
- **6 input ranges: ±200 mV up to ± 10 V**
- **Up to 64 MSample memory**
- **FIFO mode for slower samplerates**
- **Window and pulsewidth trigger**
- **Input offset up to ±100%**
- **Synchronization possible**



## Product range overview

All 16 boards of the MX.30xx series may use the on-board memory completely for the currently active number of channels.

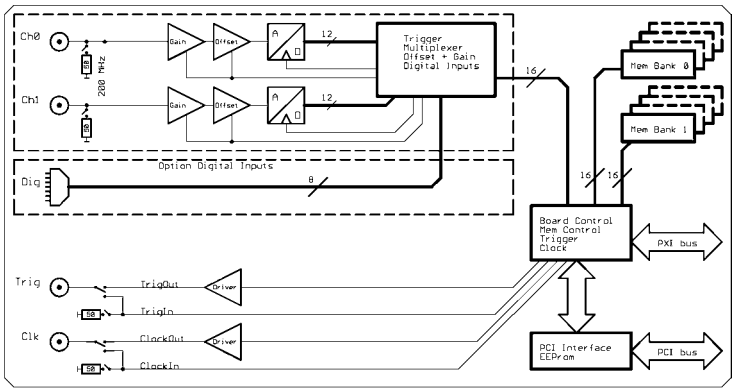
| Model | 1 channel | 2 channels |
|---|---|---|
| MX.3010 | 80 MS/s | |
| MX.3011 | 40 MS/s | 40 MS/s |
| MX.3012 | 80 MS/s | 40 MS/s |
| MX.3020 | 100 MS/s | |
| MX.3021 | 50 MS/s | 50 MS/s |
| MX.3022 | 100 MS/s | 50 MS/s |
| MX.3031 | 60 MS/s | 60 MS/s |

## Software/Drivers

A large number of drivers and examples are delivered with the board or are available as an option:

- Windows 98/ME/NT/2000/XP - drivers
- Linux - drivers
- SBench 5.2
- Streaming Software SPviewIT 6.2(as option)
- Microsoft Visual C++ examples
- Borland Delphi examples
- Microsoft Visual Basic examples
- Microsoft Excel examples
- LabWindows/CVI examples
- FlexPro support with SBench
- LabVIEW - drivers (as option)
- DASYLab - drivers (as option)
- MATLAB - drivers (as option)
- Agilent VEE - drivers (as option)

## Hardware block diagram




## Software programmable parameters

| | |
|---|---|
| Samplerate | 1 kS/s to max samplerate, external clock, ref clock, PXI clock |
| Input Range | ±200 mV, ±500 mV, ±1 V, ±2 V, ±5 V, ±10 V |
| Input impedance | 50 Ohm / 1 MOhm |
| Input Offset | ±100% in steps of 1% |
| Clock mode | internal PLL, internal quartz, external, external divided, external reference clock, PXI reference clock |
| Clock impedance | 50 Ohm / 1 MOhm |
| Trigger impedance | 50 Ohm / 1 MOhm |
| Trigger mode | Channel, External, Software, Auto, Windows, Pulse, PXI Line[5..0], PXI Startrigger |
| Trigger level | 1/256 to 255/256 of input range |
| Trigger edge | rising edge, falling edge or both edges |
| Trigger pulsewidth | 1 to 255 samples in steps of 1 sample |
| Memory depth | 32 up to installed memory in steps of 32 |
| Posttrigger | 32 up to 128 M in steps of 32 |
| Multiple Recording segmentsize | 32 up to installed memory / 2 in steps of 32 |

## Application examples

| | | |
|---|---|---|
| LDA/PDA | Production test | Laboratory equipment |
| Radar | Spectroscopie | Test of mobile communication |
| Ultrasound | Medical equipment | |

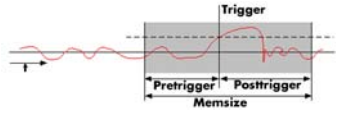
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## Possibilities and options

### Input impedance

All inputs could individually be switched by software between 50 Ohm and 1 MOhm input impedance. If using fast signals and high sampling rates or have 50 Ohm cable impedance the use of the 50 Ohm termination is recommended to minimise noise and signal reflections. If using weak signal sources or standard probes the use of the 1 MOhm termination is helpful.

### Ring buffer mode




The ring buffer mode is the standard mode of all oscilloscope boards. Data is written in a ring memory of the board until a trigger event is detected. After the event the posttrigger values are recorded. Because of this continuously recording in a ring buffer there are also samples prior to the trigger event visible: Pretrigger = Memsize - Posttrigger.

### FIFO mode

The FIFO mode is designed for continuous data transfer between measurement board and PC memory (up to 100 MB /s) or hard disk (up to 50 MB/s). The control of the data stream is done automatically by the driver on interrupt request.

### PXI bus

The PXI bus (PCI eXtension for instrumentation) offers a variety of additional normed possibilities for synchronising different components in one system. It is posible to connect several Spectrum cards with each other as well as to connect a Spectrum card with cards of other manufacturers.

### PXI reference clock

The card is able to use the 10 MHz reference clock that is supplied by the PXI system. Enabled by software the PXI reference clock is feeded in the on-board PLL. This feature allows the cards to run with a fixed phase relation.

### PXI trigger

The Spectrum cards support star trigger as well as the PXI trigger bus. using a simple software commend one or more trigger lines can be used as trigger source. This feature allows the easy setup of OR connected triggers from different cards.

### Channel trigger

The data acquisition boards offer a wide variety of trigger modes. Besides the standard signal checking for level and edge as known from oscilloscopes it's also possible to define a window trigger. All trigger modes could be combined with the pulsewidth trigger. This makes it possible to trigger on signal errors like too long or too short pulses.

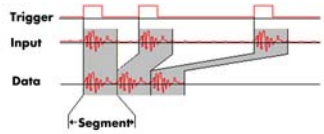
### External trigger I/O

All boards could be triggered using an external TTL signal. It's possible to use positive or negative edge also in combination with a programmable pulsewidth. An internally recognised trigger event could - activated by software - routed to the output connector to start external instruments.

### Pulse width

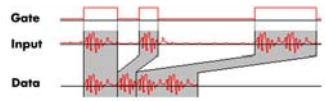
Defines the minimum or maximum width that a trigger pulse could have to generate a trigger event. Could be combined with channel trigger, pattern trigger and external trigger.

### Multiple Recording




The Multiple Recording option allows the recording of several trigger events without restarting the hardware. With this option very fast repetition rates could be achieved. The on-board memory is divided in several segments of same size. Each of them is filled with data if a trigger event occurs.

### Gated Sampling

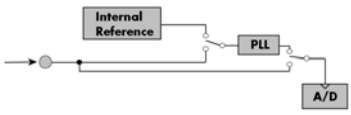



The Gated Sampling option allows data recording controlled by an external gate signal. Data is only recorded if the gate signal has a programmed level.

### External clock I/O

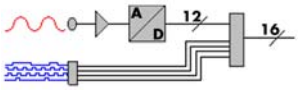
Using an external connector a sampling clock could be fed in from an external system. It's also possible to put out the internally used sampling clock to synchronise external equipment to this clock.

### Reference clock




The option to use a precise external reference clock (normally 10 MHz) is necessary to synchronise the board for high-quality measurements with external equipment (like a signal source). It's also possible to enhance the quality of the sampling clock this way. The driver automatically generates the requested sampling clock from the fed in reference clock.

### Digital inputs




This option acquires additional synchronous digital channels phase-stable with the analog data. When the option is installed there are 4 additional digital inputs for every analog A/D channel.

## Technical Data

| | | | |
|---|---|---|---|
| Resolution | 12 bit | Input signal with 50 Ohm termination | max 5 V rms |
| Differential linearity error | ≤ 1 LSB (ADC) | Input impedance | 50 Ohm / 1 MOhm \|\| 25 pF |
| Integral linearity error | ≤ 1 LSB (ADC) | Overvoltage protection (range ≤ ±1 V) | ±5 V |
| Offset error | adjustable by user | Overvoltage protection (range > ±1 V) | ±50 V |
| Gain error | < 1% | Digital Inputs input impedance | 110 Ohm @ 2.5 V |
| Crosstalk 1 MHz signal, 50 Ohm term | < -70 dB | Digital Inputs delay to analog sample | -12 samples |
| | | Dimension | 160 mm x 100 mm (3U standard) |
| Multi: Trigger to 1st sample delay | -10 to +20 samples (fix) | Width (Standard) | 1 slot |
| Multi: Recovery time | < 20 samples | Width (with digital inputs) | 2 slots |
| ext. Trigger accuracy | 1 Samples | Connector | 3 mm SMB male |
| int. Trigger accuracy | 1 Sample | Warm up time | 10 minutes |
| Trigger output delay | | Operating temperature | 0°C - 50°C |
| | | Storage temperature | -10°C - 70°C |
| Ext. clock: delay to internal clock | 42 ns ± 2 ns | Humidity | 10% to 90% |
| Min internal clock | 1 kS/s | Power consumption 5 V @ full speed | max. 2.5 A (12.5 Watt) |
| Min external clock | 1 MS/s | Power consumption 5 V @ power down | max. 1.7 A (8.5 Watt) |
| Trigger input:Standard TTL level | Low: -0.5 > level < 0.8 V<br>High: 2.0 V > level < 5.5 V<br>Trigger pulse must be valid ≥ 2 clock periods. | Clock input: Standard TTL level | Low: -0.5 > level < 0.8 V<br>High: 2.0 V > level < 5.5 V<br>Rising edge is used.<br>Required duty cycle: 50% ± 5% |
| Trigger output | Standard TTL, capable of driving 50 Ohm.<br>Low < 0.4 V (@ 20 mA, max 64 mA)<br>High > 2.4 V (@ -20 mA, max -32 mA)<br>One positive edge after the first internal trigger | Clock output | Standard TTL, capable of driving 50 Ohm<br>Low < 0.4 V (@ 20 mA, max 64 mA)<br>High > 2.4 V (@ -20 mA, max -32 mA) |

| | MX.3011 | MX.3021 | MX.3031 | MX.3010<br>MX.3012 | MX.3020<br>MX.3022 |
|---|---|---|---|---|---|
| max internal clock | 40 MS/s | 50 MS/s | 62.5 MS/s | 80 MS/s | 100 MS/s |
| max external clock | 40 MS/s | 50 MS/s | 62.5 MS/s | 80 MS/s | 100 MS/s |
| -3 dB bandwidth | > 20 MHz | > 25 MHz | > 30 MHz | > 40 MHz | > 40 MHz |
| Zero noise level | < 1.5 LSB rms | < 1.5 LSB rms | < 1.75 LSB rms | < 2.0 LSB rms | < 2.0 LSB rms |

## Dynamic Parameters

| | MX.3011 | MX.3021 | MX.3031 | MX.3010<br>MX.3012 | MX.3020<br>MX.3022 |
|---|---|---|---|---|---|
| Test - Samplerate | 40 MS/s | 50 MS/s | 60 MS/s | 80 MS/s | 100 MS/s |
| Testsignal frequency | 1 MHz | 1 MHz | 1 MHz | 1 MHz | 1 MHz |
| SNR (typ) | > 64.3 dB | > 64.3 dB | > 63.0 dB | > 64.3 dB | > 64.2 dB |
| THD (typ) | < -73.8 dB | < -73.8 dB | < -73.2 dB | < -73.8 dB | < -73.8 dB |
| SFDR (typ), incl harm. | > 77.5 dB | > 77.5 dB | > 74.3 dB | > 77.1 dB | > 76.8 dB |
| SINAD (typ) | > 63.8 dB | > 63.8 dB | > 62.6 dB | > 63.8 dB | > 63.7 dB |
| ENOB (based on SINAD) | > 10.3 LSB | > 10.3 LSB | > 10.1 LSB | > 10.3 LSB | > 10.3 LSB |

Dynamic parameters are measured at ± 1 V input range and 50 Ohm termination with the samplerate specified in the table. Measured parameters are averaged 20 times to get typical values. Test signal is a pure sine wave of the specified frequency with > 99% amplitude. SNR and RMS noise parameters may differ depending on the quality of the used PC. SNR = Signal to Noise Ratio, THD = Total Harmonic Distortion, SFDR = Spurious Free Dynamic Range, SINAD = Signal Noise and Distortion, ENOB = Effective Number of Bits. For a detailed description please see application note 002.

## Order information

| Order No | Description | Order No | Description |
|---|---|---|---|
| MX3010 | MX.3010 with 8 MSample memory and drivers/SBench 5.x | MX3xxx-16M | Option: 16 MSample memory instead of 8 MSample standard mem |
| MX3011 | MX.3011 with 8 MSample memory and drivers/SBench 5.x | MX3xxx-32M | Option: 32 MSample memory instead of 8 MSample standard mem |
| MX3012 | MX.3012 with 8 MSample memory and drivers/SBench 5.x | MX3xxx-64M | Option: 64 MSample memory instead of 8 MSample standard mem |
| MX3020 | MX.3020 with 8 MSample memory and drivers/SBench 5.x | MX3xxx-up | Additional handling costs for later memory upgrade |
| MX3021 | MX.3021 with 8 MSample memory and drivers/SBench 5.x | | |
| MX3022 | MX.3022 with 8 MSample memory and drivers/SBench 5.x | MX3xxx-mr | Option Multiple Recording: Memory segmentation |
| MX3031 | MX.3031 with 8 MSample memory and drivers/SBench 5.x | MX3xxx-gs | Option Gated Sampling: Gate signal controls acquisition |
| | | MX3xxx-dig | Additional 4 synchronous digital inputs per channel, incl. cable |
| Cab-3f-9m-80 | Adapter cable: SMB female to BNC male 80 cm | | |
| Cab-3f-9m-200 | Adapter cable: SMB female to BNC male 200 cm | MX30xx-dl | DASYLab driver for MX.30xx series |
| Cab-3f-9f-80 | Adapter cable: SMB female to BNC female 80 cm | MX30xx-hp | VEE driver for MX.30xx series |
| Cab-3f-9f-200 | Adapter cable: SMB female to BNC female 200 cm | MX30xx-lv | LabVIEW driver for MX.30xx series |
| | | MATLAB | MATLAB driver for all MI.xxxx, MC.xxxx and MX.xxxx series. |

**technical changes and printing errors possible**