SPECTRUM
SYSTEMENTWICKLUNG MICROELECTRONIC GMBH

MI.20xx - 8 bit transient recorder up to 200 MS/s

- **Standard PCI format**
- **Up to 200 MS/s on two channels**
- **Up to 100 MS/s on four channels**
- **Simultaneously sampling on all channels**
- **7 input ranges: ±50 mV up to ± 5 V**
- **Up to 512 MSample memory**
- **FIFO mode for slower samplerates**
- **Window and pulsewidth trigger**
- **Input offset up to ±400%**
- **Synchronization possible**
- **Windows program SBench 5.x included**



Product range overview

All boards of the MI.20xx series may used the on-board memory completely for the currently active number of channels.

Model	1 channel	2 channels	4 channels
MI.2020	50 MS/s	50 MS/s	
MI.2021	50 MS/s	50 MS/s	50 MS/s
MI.2030	200 MS/s	100 MS/s	
MI.2031	200 MS/s	200 MS/s	100 MS/s

Software/Drivers

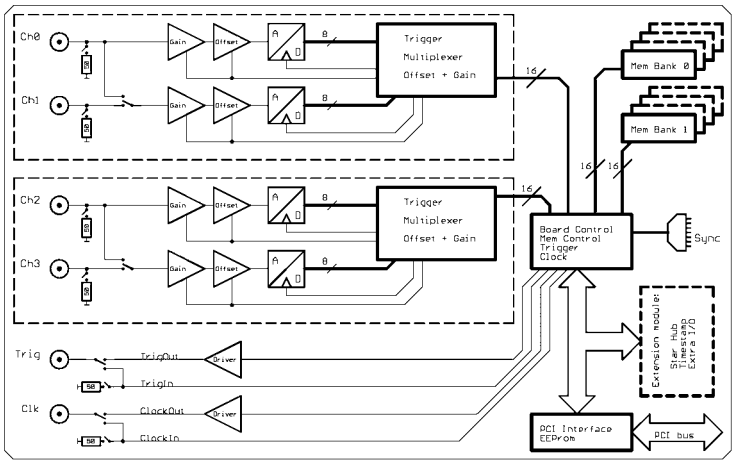
A large number of drivers and examples are delivered with the board or are available as an option:

- Windows 98/ME/NT/2000/XP - drivers
- Linux - drivers
- SBench 5.2
- Streaming Software SPviewIT 6.2(as option)
- Microsoft Visual C++ examples
- Borland Delphi examples
- Microsoft Visual Basic examples
- Microsoft Excel examples
- LabWindows/CVI examples
- FlexPro support with SBench
- LabVIEW - drivers (as option)
- DASYLab - drivers (as option)
- MATLAB - drivers (as option)
- Agilent VEE - drivers (as option)

General Information

The 4 models of the MI.20xx series are designed for the fast and high quality data acquisition. Every of the up to four input channels has its own A/D converter and its own programmable input amplifier. This allows to record signals with 8 bit resolution without any phase delay between them. The inputs could be selected to one of seven input ranges by software and could be programmed to compensate an input offset of ±400% of the input range.
The extremely large on-board memory allows long time recording even with highest samplerates. A FIFO mode is also integrated on the board. This allows to record data continuously and to process it in the PC or to store it to hard disk.

Hardware block diagram



Software programmable parameters

Samplerate	1 kS/s to max samplerate, external clock, ref clock
Input Range	±50 mV, ±100 mV, ±200 mV, ±500 mV, ±1 V, ±2 V, ±5 V
Input impedance	50 Ohm / 1 MOhm
Input Offset	±400% in steps of 1%
Clock mode	internal PLL, int.quartz, external, ext. divided, ext. reference clock
Clock impedance	50 Ohm / 1 MOhm
Trigger impedance	50 Ohm / 1 MOhm
Trigger mode	Channel, External, Software, Auto, Windows, Pulse
Trigger level	1/64 to 63/64 of input range (6 bit)
Trigger edge	rising edge, falling edge or both edges
Trigger pulsewidth	1 to 255 samples in steps of 1 sample
Memory depth	64 up to installed memory in steps of 64
Posttrigger	64 up to 128 M in steps of 64
Multiple Recording segmentsize	64 up to installed memory / 2 in steps of 64

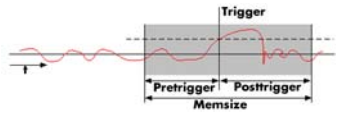
Application examples

LDA/PDA	Production test	Laboratory equipment
Radar	Spectroscopie	Test of mobile communication
Ultrasound	Medical equipment	

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Possibilities and options

Input impedance
All inputs could individually be switched by software between 50 Ohm and 1 MOhm input impedance. If using fast signals and high sampling rates or have 50 Ohm cable impedance the use of the 50 Ohm termination is recommended to minimise noise and signal reflections. If using weak signal sources or standard probes the use of the 1 MOhm termination is helpful.

Ring buffer mode


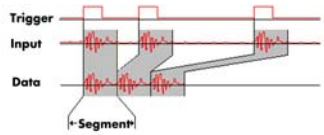
The ring buffer mode is the standard mode of all oscilloscope boards. Data is written in a ring memory of the board until a trigger event is detected. After the event the posttrigger values are recorded. Because of this continuously recording in a ring buffer there are also samples prior to the trigger event visible: Pretrigger = Memsize - Posttrigger.

FIFO mode
The FIFO mode is designed for continuous data transfer between measurement board and PC memory (up to 100 MB /s) or hard disk (up to 50 MB/s). The control of the data stream is done automatically by the driver on interrupt request.

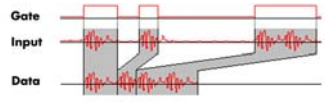
Channel trigger
The data acquisition boards offer a wide variety of trigger modes. Besides the standard signal checking for level and edge as known from oscilloscopes it's also possible to define a window trigger. All trigger modes could be combined with the pulsewidth trigger. This makes it possible to trigger on signal errors like too long or too short pulses.

External trigger I/O
All boards could be triggered using an external TTL signal. It's possible to use positive or negative edge also in combination with a programmable pulsewidth. An internally recognised trigger event could - activated by software - routed to the output connector to start external instruments.

Pulse width
Defines the minimum or maximum width that a trigger pulse could have to generate a trigger event. Could be combined with channel trigger, pattern trigger and external trigger.

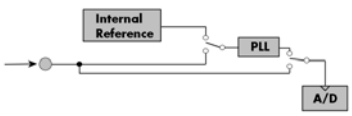
Multiple Recording


The Multiple Recording option allows the recording of several trigger events without restarting the hardware. With this option very fast repetition rates could be achieved. The on-board memory is divided in several segments of same size. Each of them is filled with data if a trigger event occurs.

Gated Sampling


The Gated Sampling option allows data recording controlled by an external gate signal. Data is only recorded if the gate signal has a programmed level.

External clock I/O
Using an external connector a sampling clock could be fed in from an external system. It's also possible to put out the internally used sampling clock to synchronise external equipment to this clock.

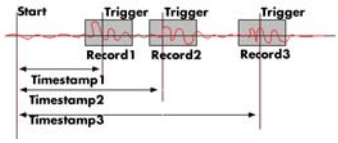
Reference clock


The option to use a precise external reference clock (normally 10 MHz) is necessary to synchronise the board for high-quality measurements with external equipment (like a signal source). It's also possible to enhance the quality of the sampling clock this way. The driver automatically generates the requested sampling clock from the fed in reference clock.

Cascading
The cascading option synchronises up to 4 Spectrum boards internally. It's the simpliest way to build up a multi channel system. There is a phase delay between two boards of about 500 pico seconds when this synchronisation option is used.

Star hub
The star hub is an additional module allowing the phase stable synchronisation of up to 16 boards. Independent of the number of boards there is no phase delay between all channels. The star hub distributes trigger and clock information between all boards. As a result all connected boards are running with the same clock and the same trigger.

Extra I/O
The Extra I/O module adds 24 additional digital I/O lines and 4 analog outputs on an extra connector. These additional lines are independent from the standard function and could be controlled asynchronously. There is also an internal version available with 16 digital I/Os and 4 analog outputs that could be used directly at the rear board connector.

Timestamp


The timestamp option writes the time positions of the trigger events in an extra memory. The timestamps are relatively to the start of recording, to a defined zero time or externally synchronised to a radio clock or a GPS receiver. With this option acquisitions of systems on different locations could be set in a precise time relation.

Technical Data

Resolution	8 bit	Dimension	312 mm x 107 mm
Differential linearity error (ADC)	0.5 LSB typ.	Width (Standard)	1 full size slot
Integral linearity error (ADC)	0.5 LSB typ.	Width (with star hub option)	2 full size slots
Multi: Trigger to 1st sample delay	fixed	Analogue Connector	3 mm SMB male
Multi: Recovery (re-arm) time	< 20 samples	Overvoltage protection (range < ±500 mV)	±5 V
Trigger accuracy 2/4 channel mode	1 Sample	Overvoltage protection (range > ±500 mV)	±50 V
Trigger accuracy 1 channel mode	2 Samples	Warm up time	10 minutes
Ext. clock: delay to internal clock	42 ns ± 2 ns	Operating temperature	0°C - 50°C
input signal with 50 ? termination	max 5 V rms	Storage temperature	-10°C - 70°C
Trigger output delay	1 Sample	Humidity	10% to 90%
Input impedance	50 Ohm / 1 MOhm || 25 pF		
Min internal clock	1 kS/s	Power consumption 5 V @ full speed	max 3.4 A (17.0 Watt)
Min external clock	1 MS/s	Power consumption 5 V @ power down	max 1.9 A (9.5 Watt)
Trigger input:Standard TTL level	Low: -0.5 > level < 0.8 V High: 2.0 V > level < 5.5 V Trigger pulse must be valid ≥ 2 clock periods.	Clock input: Standard TTL level	Low: -0.5 > level < 0.8 V High: 2.0 V > level < 5.5 V Rising edge is used. Required duty cycle: 50% ± 5%
Trigger output	Standard TTL, capable of driving 50 Ohm. Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -32 mA) One positive edge after the first internal trigger	Clock output	Standard TTL, capable of driving 50 Ohm Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -32 mA)

Input range	±50 mV	±100 mV	±200 mV	±500 mV	±1 V	±2 V	±5 V
Software programmable offset	±200 mV	±400 mV	±800 mV	±2 V	±4 V	±8 V	±20 V
Offset error	< 1 LSB, adjustable by user						
Gain error	< 2 %	< 2 %	< 2 %	< 2 %	< 2 %	< 2 %	< 2 %
MI.202x: Noise (rms): 50 Ohm, 50 MS/s	< 0.5 LSB	< 0.5 LSB	< 0.5 LSB	< 0.5 LSB	< 0.5 LSB	< 0.5 LSB	< 0.5 LSB
MI.203x: Noise (rms): 50 Ohm, 100/200 MS/s	< 2.0 LSB	< 1.5 LSB	< 1.0 LSB	< 1.0 LSB	< 1.0 LSB	< 1.0 LSB	< 1.0 LSB
Crosstalk 5 MHz signal, ±50 mV input, 50 Ohm	< 62 dB						

	MI.2020 MI.2021	MI.2030 MI.2031
max internal clock	50 MS/s	200 MS/s
max external clock	50 MS/s	100 MS/s
-3 dB bandwidth	> 25 MHz	> 90 MHz

Dynamic Parameters

	MI.2020 MI.2021	MI.2030 MI.2031
Test - Samplerate	50 MS/s	100 MS/s
Testsignal frequency	1 MHz	1 MHz
SNR (typ)	> 47.5 dB	> 45.9 dB
THD (typ)	< -52.5 dB	< -49.1 dB
SFDR (typ), incl harm.	> 57.0 dB	> 55.5 dB
SINAD (typ)	> 46.0 dB	> 44.2
ENOB (based on SINAD)	> 7.3	> 7.1

Dynamic parameters are measured at ± 1 V input range and 50 Ohm termination with the samplerate specified in the table. Measured parameters are averaged 20 times to get typical values. Test signal is a pure sine wave of the specified frequency with > 99% amplitude. SNR and RMS noise parameters may differ depending on the quality of the used PC. SNR = Signal to Noise Ratio, THD = Total Harmonic Distortion, SFDR = Spurious Free Dynamic Range, SINAD = Signal Noise and Distortion, ENOB = Effective Number of Bits. For a detailed description please see application note 002.

Order information

Order No	Description	Order No	Description
MI2020	MI.2020 with 16 MSample memory and drivers/SBench 5.x	MI2xxx-32M	Option: 32 MSample memory instead of 16 MSample standard mem
MI2021	MI.2021 with 16 MSample memory and drivers/SBench 5.x	MI2xxx-64M	Option: 64 MSample memory instead of 16 MSample standard mem
MI2030	MI.2030 with 16 MSample memory and drivers/SBench 5.x	MI2xxx-128M	Option: 128 MSample memory instead of 16 MSample standard mem
MI2031	MI.2031 with 16 MSample memory and drivers/SBench 5.x	MI2xxx-256M	Option: 256 MSample memory instead of 16 MSample standard mem
		MI2xxx-512M	Option: 512 MSample memory instead of 16 MSample standard mem
MI2xxx-smod	Star Hub: Synchronisation of 2 - 16 boards, one option per system	MI2xxx-up	Additional handling costs for later memory upgrade
MIxxxx.xio	Extra I/O, internal connector: 16 DI/O, 4 Analog out		
MIxxxx-xmf	Extra I/O, external connector: 24 DI/O, 4 Analog out, incl. cable	MI2xxx-mr	Option Multiple Recording: Memory segmentation
MI2xxx-time	Timestamp option: Extra memory for trigger time	MI2xxx-gs	Option Gated Sampling: Gate signal controls acquisition
		MI2xxx-cs	Synchronisation of 2 - 4 boards, one option per system
Cab-3f-9m-80	Adapter cable: SMB female to BNC male 80 cm		
Cab-3f-9m-200	Adapter cable: SMB female to BNC male 200 cm	MI20xx-dl	DASYLab driver for MI.20xx series
Cab-3f-9f-80	Adapter cable: SMB female to BNC female 80 cm	MI20xx-hp	VEE driver for MI.20xx series
Cab-3f-9f-200	Adapter cable: SMB female to BNC female 200 cm	MI20xx-lv	LabVIEW driver for MI.20xx series
		MATLAB	MATLAB driver for all MI.xxxx, MC.xxxx and MX.xxxx series.