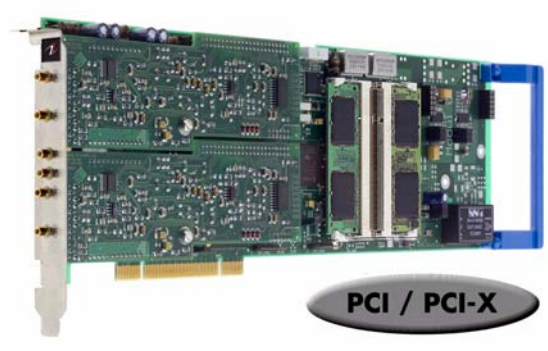
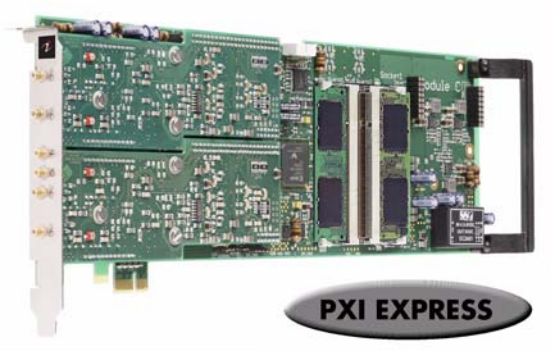
UF2-3100 : 8 channel 12 bit Digitizer / Transient Recorder to 25 MS/s, PCI

- **Multi channel 12 bit A/D converter board**
- **2, 4 or 8 channels with 1 MS/s, 10 MS/s and 25 MS/s**
- **Simultaneous sampling on all channels**
- **Separate ADC and amplifier per channel**
- **8 input ranges: ±50 mV up to ±10 V**
- **Up to 2 GSample (4 GByte) on-board memory**
- **128 MSample standard memory installed**
- **Window, pulse width, re-arm, OR/AND trigger**
- **Programmable input offset of ±100%**
- **Synchronization of up to 16 cards per system and up to 271 cards in multiple PC's**
- **Options: synchronous digital channels, ABA mode, BaseXIO**





- UF2-3100 series
- 66 MHz 32 Bit PCI-X interface
- 5V / 3.3V PCI compatible
- 100% compatible to conventional PCI > V2.1
- Sustained streaming mode up to 225 MB/s

- UF2e-3100 series
- 2.5 GBit x1 PCIe Interface
- Works with x1/x4/x8/x16* PCIe slots
- Software compatible to PCI
- Sustained streaming mode up to 160 MB/s

Operating Systems	**Recomended Software**	**Drivers**
• Windows 2k, XP, Vista • Linux Kernel 2.4 + 2.6 • Both 32 and 64 bit	• Visual Basic, Visual C++, Borland C++ Builder, GNU C++, Borland Delphi, .VB.NET, C#, J# • SBench, SPviewIT	• MATLAB • LabVIEW, LabWindows • DASY*Lab* • Agilent VEE

Model	1 channel	2 channels	4 channels	8 channels
UF2-3110	1 MS/s	1 MS/s		
UF2-3111	1 MS/s	1 MS/s	1 MS/s	
UF2-3112	1 MS/s	1 MS/s	1 MS/s	1 MS/s
UF2-3120	10 MS/s	10 MS/s		
UF2-3121	10 MS/s	10 MS/s	10 MS/s	
UF2-3122	10 MS/s	10 MS/s	10 MS/s	10 MS/s
UF2-3130	25 MS/s	25 MS/s		
UF2-3131	25 MS/s	25 MS/s	25 MS/s	
UF2-3132	25 MS/s	25 MS/s	25 MS/s	25 MS/s

General Information

The UF2-3100 and UF2e-3100 series are designed for the fast and high quality data acquisition. Each channel has it's own 12-bit ADC for simultaneous sampling together with an amplifier, input impedance of 50 Ohm or 1 MOhm and programmable offset - so that each channel can be setup to best match the input signal.
All UF2 and UF2e cards support recording to card memory and off-load at the end of the measurement, or continuous streaming to the host PC. When some channels are not used, all of the card memory is available to the active channels. External clock and trigger connectors enable synchronization with external equipment. The user is able to select from 7 external trigger modes and 20 internal trigger modes to ensure that the critical signals are recorded. The fine resolution clock can be further enhanced with a user-specified quartz oscillator as a cost-option when precise sample rates are required. The Multiple Recording (memory segmentation), Gated Sampling and Timestamp options are popular requests for RADAR and Ultrasound projects. Pedigree : the first high-speed PC instrument was made in 1989.

*Some x16 PCIe slots are for the use of graphic cards only and can not be used for other cards.

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Software Support

Windows drivers

The cards are delivered with drivers for Windows 2000, XP, XP64, Vista and Vista64. Programming examples for Visual C++, Borland C++ Builder, LabWindows/CVI, Borland Delphi, Visual Basic, VB.NET, C# and J# are included.

Linux Drivers

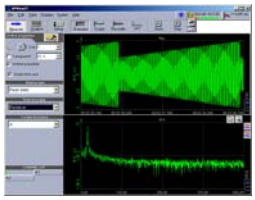


All cards are delivered with full Linux support. Pre compiled kernel modules are included for the most common distributions like RedHat, Fedora, Suse or Debian. The Linux support includes SMP systems, 32 bit and 64 bit systems, versatile programming examples for Gnu C++ as well as the possibility to get the driver sources for own compilation.

SBench

A full licence of the SBench measurement and waveform generation software for the UltraFast cards is included in the delivery. Version 6 is running under Windows as well as under Linux (KDE and GNOME).

SPViewIT



SPviewIT is the professional streaming software solution for the Strategic Test PC instruments. The software is optimised for continuous data acquisition of large amounts of data. Key features of SPviewIT are different data displays, editable interface and a wide choice of export filters. A demo version comes with the card.

Third-party products

Additional drivers are available as a cost-option for LabVIEW, MATLAB, DASYLab and Agilent VEE. All drivers are supplied with examples and detailed documentation.

UF Software compatibility layer

For existing customers of the older UF series cards, a special software compatibility layer is provided for the UF2/UF2e cards. This DLL converts UF calls to UF2 calls and simulates a UF card in the software.

Hardware features and options

PCI/PCI-X



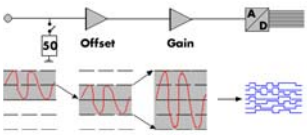
The UF2 cards with PCI/PCI-X bus connector use 32 Bit and up to 66 MHz clock rate for data transfer. They are 100% compatible to Conventional PCI > V2.1. The universal interface allow their use in PCI slots with 5 V I/O and 3.3 V I/O voltages as well as in PCI-X or PCI 64 slots. The maximum sustained data transfer rate is 225 MByte/s per bus segment.

PCI Express



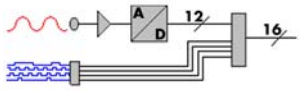
The UF2e cards with PCI Express use a x1 PCIe connector. They can be used in PCI Express x1/x4/x8/x16 slots, except special graphic card slots, and are 100% software compatible to Conventional PCI > V2.1. The maximum sustained data transfer rate is 160 MByte/s per slot.

Input Amplifier



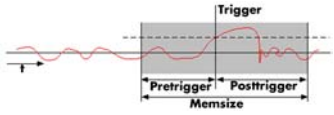
The analog inputs can be adapted to real world signals using a wide variety of settings that are individual for each channel. By using software commands the input termination can be changed between 50 Ohm and 1 MOhm, one can select a matching input range and the signal offset can be compensated for.

Digital inputs



This option acquires additional synchronous digital channels phase-stable with the analog data. When the option is installed there are 4 additional digital inputs for every analog A/D channel.

Ring buffer mode



The ring buffer mode is the standard mode of all oscilloscope boards. Data is written in a ring memory of the board until a trigger event is detected. After the event the posttrigger values are recorded. Because of this continuous recording into a ring buffer the samples prior to the trigger event are visible: Pretrigger = Memsize - Posttrigger.

FIFO mode

The FIFO (streaming) mode is designed for continuous data transfer between measurement board and PC memory (up to 225 MB/s on a PCI-X slot and up to 160 MB/s on evry PCI Express slot) or hard disk. The control of the data stream is done automatically by the driver on interrupt request. TAll of the installed on-board memory is used for buffer data, making the continuous streaming extremely reliable.

Channel trigger

The data acquisition boards offer a wide variety of trigger modes. Besides the standard signal checking for level and edge known from oscilloscopes it's also possible to define a window trigger. All trigger modes can be combined with the pulsewidth trigger. This makes it possible to trigger on signal errors like too long or too short pulses. In addition to this a re-arming mode (for accurate trigger recognition on noisy signals) and an AND/OR combination of different trigger events is possible. As a unique feature it is possible to use deactivated channels as trigger sources.

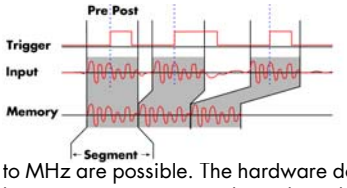
External trigger I/O

All boards can be triggered using an external TTL signal. It's possible to use positive or negative edge also in combination with a programmable pulse width. An internally recognised trigger event can - when activated by software - be routed to the trigger connector to start external instruments.

Pulse width

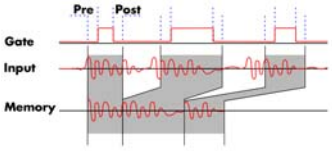
Defines the minimum or maximum width that a trigger pulse must have to generate a trigger event. Pulse width can be combined with channel trigger, pattern trigger and external trigger.

Multiple Recording



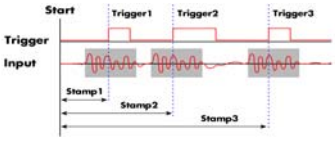
The Multiple Recording option allows the recording of several trigger events with an extremely short re-arming time of less than 4 samples. Pulse Repetition Frequencies to MHz are possible. The hardware doesn't need to be restarted in between trigge revents. The on-board memory is divided in several segments of the same size. Each of them is filled with data if a trigger event occurs. Pre- and posttrigger of the segments can be programmed. The number of acquired segments is only limited by the used memory and is unlimited when using FIFO mode.

Gated Sampling



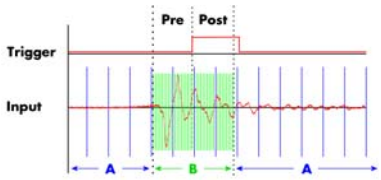
The Gated Sampling option allows data recording controlled by an external gate signal. Data is only recorded if the gate signal has a programmed level. In addition a pre-area before start of the gate signal as well as a post area after end of the gate signal can be acquired. The number of gate segments is only limited by the used memory and is unlimited when using FIFO mode.

Timestamp



The timestamp option writes the time positions of the trigger events in an extra memory. The timestamps are relative to the start of recording, a defined zero time, externally synchronised to a radio clock, or a GPS receiver. With this option acquisitions of systems on different locations can be set in a precise time relation.

ABA mode

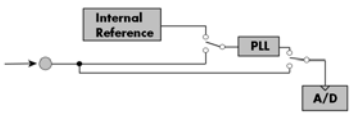


The optional ABA mode combines slow continuous data recording with fast acquisition on trigger events. The ABA mode works like a slow data logger combined with a fast digitizer. The exact position of the trigger events is stored as timestamps in an extra memory.

External clock I/O

Using a dedicated connector a sampling clock can be fed in from an external system. It's also possible to output the internally used sampling clock to synchronise external equipment to this clock.

Reference clock



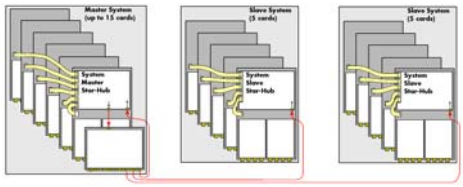
The option to use a precise external reference clock (normally 10 MHz) is necessary to synchronise the board for high-quality measurements with external equipment (like a signal source). It's also possible to enhance the quality of the sampling clock in this way. The driver automatically generates the requested sampling clock from the fed in reference clock.

Star-Hub



The Star Hub is an additional module allowing the phase stable synchronisation of up to 16 boards in one system. Regardless of the number of boards there is no phase delay between all channels. The Star Hub distributes trigger and clock information between all boards. As a result all connected boards are running with the same clock and the same trigger. All trigger sources can be combined with OR/AND allowing all channels of all cards to be trigger source at the same time. The Star Hub is available as 5 card and 16 card version. The 5 card version doesn't need an extra slot width.

271 synchronous cards with theSystem Star-Hub



With the help of multiple System Star-Hubs it is possible to link up to 17 system phase synchronous with each other. Each system can then contain up to 16 cards (master only 15). In total 271 cards can be used fully synchronously in multiple PC's. One master system distributes clock and trigger signal to all connected slave systems.

BaseXIO (enhanced trigger)



The BaseXIO option offers 8 asynchronous digital I/O lines on the base card. The direction can be selected by software in groups of four. Two of these lines can also be used as additional external trigger sources. This allows the building of complex trigger combinations with external gated triggers as well as AND/OR combination of multiple external trigger sources - for example, the picture and row synchronisation of video signals. In addition one of the I/O lines can be used as reference clock for the Timestamp counter.

Technical Data

Analog Inputs

Resolution	12 bit
Differential non linearity (DNL)	≤ 1 LSB (ADC)
Integral non linearity (INL)	≤ 2.5 LSB (ADC)
Offset error	can be calibrated by user
Gain error	< 1% of current value
Programmable input offset	±100% of current input range
Crosstalk: ±50 mV, 50 Ohm, 500 kHz	< -70 dB between any adjacent channels
Input signal with 50 Ohm termination	max 5 V rms
Analog Input impedance	50 Ohm / 1 MOhm || 25 pF
Over voltage protection (range ≤ ±1 V)	±5 V
Over voltage protection (range > ±1 V)	±50 V
Connector (analog and trigger/clock)	3 mm SMB male

Trigger

Multi, Gate: re-arming time	<4 Samples
Max Pretrigger at Multi, Gate, FIFO	8176 Samples as sum of all active channels
Internal/External trigger accuracy	1 Sample
Channel trigger resolution	10 bits
Trigger output delay	One positive edge after internal trigger event
External trigger type	3.3V LVTTL compatible (5V tolerant)
External trigger input	Low ≤ 0.8 V, High ≥ 2.0 V, ≥ 2 clock periods
External trigger maximum voltage	-0.5 V up to +5.7 V (internally clamped to 5.0V, 100 mA max. clamping current)
External trigger output levels	Low ≤ 0.4 V, High ≥ 2.4 V, TTL compatible
External trigger output drive strength	Capable of driving 50 ohm load

Digital Inputs (Option)

Digital inputs: input impedance	110 Ohm @ 2.5V
Digital inputs delay to analog sample	-4 samples (digital 4 samples before analog)
Maximum voltage	-0.3 V up to +5.5 V
Input voltage	Low ≤ 0.8 V, High ≥ 2.0 V
Connector (digital inputs)	40 pole half pitch (Hirose FX2 series)

BaseXIO (Option)

BaseXIO Connector (extra bracket)	8 x SMB (8 x MMCX internal)
BaseXIO input	TTL compatible: Low ≤ 0.8 V, High ≥ 2.0 V
BaseXIO input maximum voltage	-0.5 V up to +5.5 V
BaseXIO output levels	TTL compatible: Low ≤ 0.4 V, High ≥ 2.4 V
BaseXIO output drive strength	32 mA maximum current

Power consumption (max speed)	**PCI / PCI-X**		**PCI EXPRESS**	
	3,3 V	**5 V**	**3,3 V**	**12 V**
UF2-31x0 (128 MS)	2.1 A	0.7 A	0,4 A	0,9 A
UF2-31x1 (128 MS)	2.3 A	0.9 A	0,4 A	1,00 A
UF2-31x2 (128 MS)	2.7 A	1.6 A	0,4 A	1,5 A
M2i-3132 (2 GS), max power	3.8 A	1.6 A	0,4 A	2,1 A

Max channels with Star-Hub	**SH5**	**SH16**	**SSHS5**	**SSHS16**
UF2-31x0	10	32	170	542
UF2-31x1	20	64	340	1084
UF2-31x2	40	128	680	2168

Certifications and Compliances

EMC Immunity	Compliant with CE Mark
EMC Emission	Compliant with CE Mark

Clock

Internal clock range (PLL mode)	1 kS/s to max (see table below)
Internal clock accuracy	20 ppm
Internal clock: max. jitter in PLL mode	TBD
Internal clock: max. jitter in quartz mode	TBD
Internal clock setup granularity	≤1% of range (100M, 10M, 1M, 100k,...
Internal clock setup granularity example	range 1M to 10M: stepsize ≤ 100k
Reference clock: external clock range	≥ 1.0 MHz and ≤ 125.0 MHz
External clock range	1 kS/s to max (see table below)
External clock delay to internal clock	5.4 ns
External clock type	3.3V LVTTL compatible
External clock input	Low ≤ 0.8 V, High ≥ 2.0 V, duty 45% - 55%
External clock maximum voltage	-0.5 V up to +3.8 V (internally clamped to 3.3V, 100 mA max. clamping current)
External clock output levels	Low ≤ 0.4 V, High ≥ 2.4 V, TTL compatible
External clock output drive strength	Capable of driving 50 ohm load

Environmental and Physical details

Dimension (PCB only)	312 mm x 107 mm (full PCI length)
Width (Standard or star-hub 5)	1 full size slot
Width (star-hub 16)	2 full size slots
Width (with digital inputs)	1 full size slots + 1 half size slot
Weight (depending on options/channels)	290g (2/4 ch) up to 460g (8 ch + dig + sh)
Warm up time	10 minutes
Operating temperature	0°C - 50°C
Storage temperature	-10°C - 70°C
Humidity	10% to 90%

PCI / PCI-X specific details

PCI / PCI-X bus slot type	32 bit 33/66 MHz
PCI / PCI-X bus slot compatibility	32/64 bit, 33-133 MHz, 3,3 V and 5 V I/O

PCI EXPRESS specific details

PCIe slot type	x1
PCIe slot compatibility	x1/x4/x8/x16*

*Some x16 PCIe slots are for graphic cards only and can not be used for other cards.

Software programmable parameters

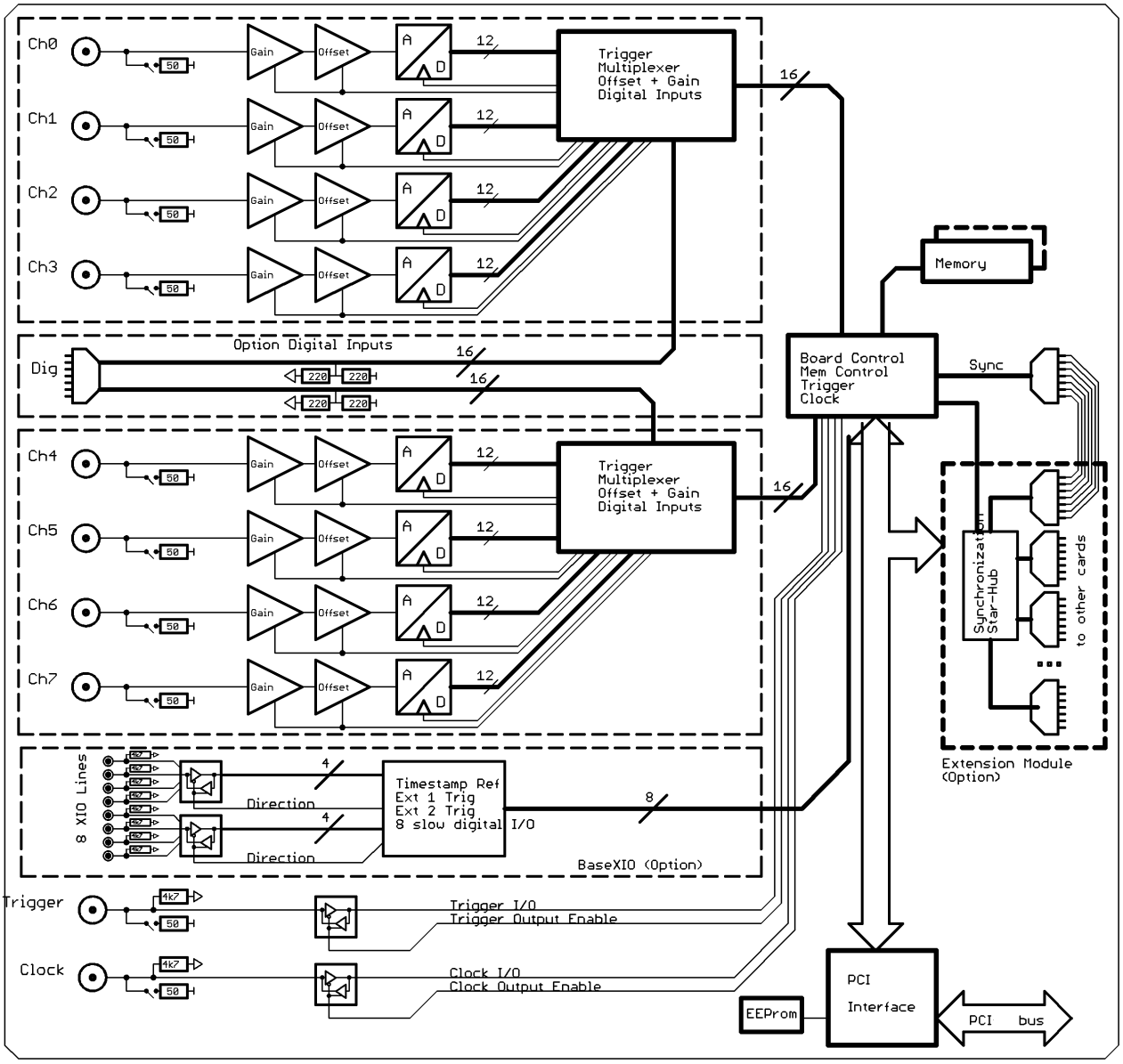
Input Range	±50 mV, ±100 mV, ±200 mV, ±500 mV, ±1 V, ±2 V, ±5 V, ±10 V
Input impedance	50 Ohm / 1 MOhm
Input Offset	±100% of input range in steps of 1%
Clock mode	Int. PLL, int. quartz, ext. clock, ext. divided, ext. reference clock, sync
Clock impedance	50 Ohm / high impedance (> 4kOhm)
Trigger impedance	50 Ohm / high impedance (> 4kOhm)
Trigger mode	Channel, Extern, SW, Auto, Window, Pulse, Re-Arm, Or/And, Delay
Trigger level resolution	10 bit resolution: 1/1024 to 1023/1024 of input range
Trigger edge	Rising edge, falling edge or both edges
Trigger pulse width	0 to [64k - 1] samples in steps of 1 sample
Trigger delay	0 to [64k - 1] samples in steps of 1 sample
Memory depth	8 up to [installed memory / number of active channels] in steps of 4
Posttrigger	4 up to [8G - 4] samples in steps of 4
Multiple Recording segment size	8 up to[installed memory / 2 / active channels] in steps of 4
Multi / Gated pretrigger	0 up to [8k samples / number of active channels - 16]
ABA clock divider	1 up to [64k - 1] in steps of 1
Synchronization clock divider	2 up to [8k - 2] in steps of 2
Channel selection	Any number of available channels (see manual for selection limits)

Dynamic Parameters

UF2/UF2e	-3110 -3111		-3112		-3120 -3121		-3122		-3130 -3131		-3132	
max internal clock	1 MS/s		1 MS/s		10 MS/s		10 MS/s		25 MS/s		25 MS/s	
max external clock	1 MS/s		1 MS/s		10 MS/s		10 MS/s		25 MS/s		25 MS/s	
-3 dB bandwidth	DC to 500 kHz		DC to 500 kHz		DC to 5 MHz		DC to 5 MHz		DC to 12.5 MHz		DC to 12.5 MHz	
Zero noise level (range ≤ ±100 mV)	0.9 LSB rms		1.0 LSB rms		1.6 LSB rms		1.7 LSB rms		1.7 LSB rms		2.0 LSB rms	
Zero noise level (range > ±100 mV)	0.7 LSB rms		0.8 LSB rms		1.1 LSB rms		1.2 LSB rms		1.2 LSB rms		1.2 LSB rms	
Test - sampling rate	1 MS/s		1 MS/s		10 MS/s		10 MS/s		25 MS/s		25 MS/s	
Test signal frequency	10 kHz	90 kHz	10 kHz	90 kHz	90 kHz	1 MHz	90 kHz	1 MHz	1 MHz	4 MHz	1 MHz	4 MHz
SNR (typ)	66.7 dB	66.1 dB	66.5 dB	66.1 dB	66.0 dB	65.3 dB	65.5 dB	65.0 dB	63.5 dB	62.5 dB	63.5 dB	62.5 dB
THD (typ)	-63.1 dB	-62.9 dB	-63.1 dB	-62.9 dB	-63.0 dB	-62.8 dB	-63.0 dB	-62.8 dB	-62.2 dB	-61.5 dB	-62.3 dB	-61.0 dB
SFDR (typ), excl. harm.	82.7 dB	81.5 dB	82.7 dB	81.5 dB	82.5 dB	79.5 dB	82.5 dB	79.5 dB	81.3 dB	79.0 dB	79.2 dB	78.5 dB
ENOB (based on SINAD)	9.9 bit	9.8 bit	9.9 bit	9.8 bit	9.9 bit	9.8 bit	9.8 bit	9.7 bit	9.6 bit	9.5 bit	9.6 bit	9.5 bit
ENOB (based on SNR)	10.7 bit	10.6 bit	10.7 bit	10.6 bit	10.6 bit	10.5 bit	10.5 bit	10.4 bit	10.2 bit	10.1 bit	10.2 bit	10.1 bit

Dynamic parameters are measured at ± 1 V input range (if no other range is stated) and 50 Ohm termination with the samplerate specified in the table. Measured parameters are averaged 20 times to get typical values. Test signal is a pure sine wave of the specified frequency with > 99% amplitude. SNR and RMS noise parameters may differ depending on the quality of the used PC. SNR = Signal to Noise Ratio, THD = Total Harmonic Distortion, SFDR = Spurious Free Dynamic Range, SINAD = Signal Noise and Distortion, ENOB = Effective Number of Bits. For a detailed description please see application note 002.

Hardware block diagram



Order Information

Versions

Order no.	Standard mem	1 channel	2 channels	4 channels	8 channels
UF2-3110, UF2e-3110	128 MSample	1 MS/s	1 MS/s		
UF2-3111, UF2e-3111	128 MSample	1 MS/s	1 MS/s	1 MS/s	
UF2-3112, UF2e-3112	128 MSample	1 MS/s	1 MS/s	1 MS/s	1 MS/s
UF2-3120, UF2e-3120	128 MSample	10 MS/s	10 MS/s		
UF2-3121, UF2e-3121	128 MSample	10 MS/s	10 MS/s	10 MS/s	
UF2-3122, UF2e-3122	128 MSample	10 MS/s	10 MS/s	10 MS/s	10 MS/s
UF2-3130, UF2e-3130	128 MSample	25 MS/s	25 MS/s		
UF2-3131, UF2e-3131	128 MSample	25 MS/s	25 MS/s	25 MS/s	
UF2-3132, UF2e-3132	128 MSample	25 MS/s	25 MS/s	25 MS/s	25 MS/s

Memory

Order no.	Option
UF2-3100-256MS	Memory upgrade to 512 MB of total memory
UF2-3100-512MS	Memory upgrade to 1 GB of total memory
UF2-3100-1GS	Memory upgrade to 2 GB of total memory
UF2-3100-2GS	Memory upgrade to 4 GB of total memory

Options

Order no.	Option
UF2-3100-mr	Option Multiple Recording
UF2-3100-mgt	Option pack including Multiple Recording, Gated Sampling, Timestamp
UF2-3100-mgtab	Option pack including Multiple Recording, Gated Sampling, Timestamp, ABA mode
UF2-3100-SH5 (1)	Synchronization Star-Hub for up to 5 cards, only 1 slot width
UF2-3100-SH16 (1)	Synchronization Star-Hub for up to 16 cards
UF2-3100-SSHM (1)	System-Star-Hub Master for up to 15 cards in the system and up to 17 systems, sync cables included
UF2-3100-SSHS5 (1)	System-Star-Hub Slave for up to 5 cards in one system, all sync cables included
UF2-3100-SSHS16 (1)	System-Star-Hub Slave for up to 16 cards in one system, all sync cables included
UF2-3100-dig	Additional synchronous digital inputs (4 per analog channel) including Cab-d40-idc-100
UF2-3100-bxio	Option BaseXIO: 8 digital I/O lines usable as asynchronous I/O, timestamp ref-clock and additional external trigger lines, additional bracket with 8 SMB connectors
UF2-upgrade	Upgrade for UF2 or UF2e; later installation of option -dig or -bxio

Cables

Order no.	Option
Cab-3f-9m-80	Adapter cable SMB female to BNC male, 80 cm
Cab-3f-9f-80	Adapter cable SMB female to BNC female, 80 cm
Cab-3f-3f-80	Adapter cable SMB female to SMB female, 80 cm
Cab-3f-9m-200	Adapter cable SMB female to BNC male, 200 cm
Cab-3f-9f-200	Adapter cable SMB female to BNC female, 200 cm
Cab-3f-3f-200	Adapter cable SMB female to SMB female, 200 cm
Cab-3f-9f-5	Adapter cable SMB female to BNC female, 5 cm (short cable especially for oscilloscopes probes)
Cab-d40-idc-100	Flat ribbon cable 40 pole FX2 for digital connector to -2x20 pole IDC connector, 100 cm
Cab-d40-d40-100	Flat ribbon cable 40 pole FX2 for digital connector to 40 pole digital FX2 connector, 100 cm

Drivers

Order no.	Option
UF2-ml	MATLAB driver for all UF2 and UF2e cards
UF2-3100-lv	LabVIEW driver for all UF2-3100 and UF2e-3100 cards
UF2-3100-dl	DASYLab driver for all UF2-3100 and UF2e-3100 cards
UF2-3100-vee	Agilent VEE driver for all UF2-3100 and UF2e-3100 cards

(1) : Only one of the options can be installed on a card at a time.

Warranty and Software Maintenance

All UltraFast boards are supplied with a two-year hardware warranty and include life-time technical support and free software updates. This includes SDK's for future Microsoft Windows and Linux versions and third-party software drivers.

technical changes and printing errors possible