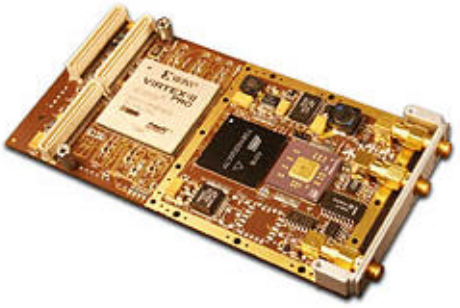
ADC3200 — 2GS/s, 1-Ch, 10-Bit PMC

Features



- **2 GS/s, 10-bit vertical resolution**
- **Bandwidth 3GHz**
- **192M Byte SDRAM Buffer**
- **SNR Minimum 44dB**
- **Xilinx Virtex II Pro FPGA XC2VP20/50**
- **SMA Connectors on all signals**
- **Software Drivers for VxWorks, Windows and Linux.**

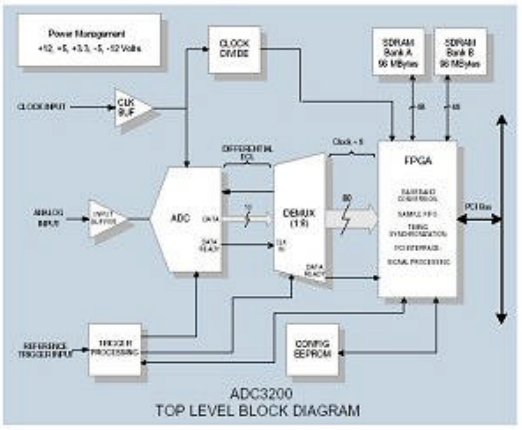
Description

The ADC3200 is a 2GHz PMC analog to digital converter module with on-board digital filtering, designed for digitizing wide bandwidth analog signals at sampling rates of up to 2GS/s. Buffering of the digitized data samples is provided onboard, as well as in-phase and quadrature data processing.
A Xilinx Virtex II Pro FPGA provides preprocessing, continuous sampling, digital filtering, buffering and timing. A variety of FPGA functions for ADC3200 has been developed including:
I/Q Generation/demodulation, Digital Down-Conversion, FIR Filter, FFT, and more.

For PC-based systems under Windows, a visualization application (ADCView) is provided which displays samples data graphically in real-time.
Through ADCView's graphical user interface, users can configure sampling parameters such as: start and stop vectors and external triggering.
The ADC3200 is a PMC based technology that has been rigorously tested to operate on leading PowerPC, PC and DSP host processor systems.

Interfaces

Analog Input
An analog single-ended input signal is accepted through an SMA female type connector on the front edge of the module.
Clock Input and Output
An analog single-ended clock input of +4dBm is provided through an SMA female type connector on the front edge of the module. The signal input is looped through to an output.
Trigger Input
Trigger input is provided through an SMA female type connector on the front of the module.
PCI Interface
Processed sample data is transferred to the host system through the PCI bus. Data collection timing and duration are fully programmable through the PCI bus. PCI interface is implemented in an onboard FPGA.
JTAG Interface
In-system reprogramming of the FPGA is provided by a JTAG interface.
FPGA Customization
The board's Xilinx Virtex II Pro family FPGA implements processing, buffering, timing, and the PCI interface.
FPGA design can be customized for specific applications such as data preprocessing and DSP functions such as FIR, FFT, and IQ Demodulation.



ADC3200
TOP LEVEL BLOCK DIAGRAM

Applications

- Radar design and testing
- LIDAR
- SATCOM
- Data Analysis System
- Direct RF down conversion
- High Energy Physics

Analog ADC Performance
3.0 GHz Full Power Input Bandwidth (-3 dB)
Band Flatness: ± 0.2 dB (from DC up to 1.5 GHz)
SFDR = 58 dBc ; 7.4 Effective Bits @ FS = 1.4 GSPS, FIN = 700 MHz [-1dBFS]
SFDR = 48 dBc ; 7.2 Effective Bits @ FS = 1.4 GSPS, FIN = 1950 MHz [-1dBFS]
SFDR = 46 dBc ; 6.2 Effective Bits @ FS = 2 GSPS, FIN = 950 MHz [-1dBFS]

Power Requirements
+12V 0.60 Amps
+5V 0.05 Amps
+3.3V 3.16 Amps
-12V 0.84 Amps
Total Card Dissipation
DRAM Disabled: 17 Watts
DRAM Enabled: 21.6 Watts

Environmental Requirements
Operating Temperature
Commercial Version: 0°C to 50°C
Industrial Version: -40°C to 70°C
400 LFM Minimum Air Flow Required